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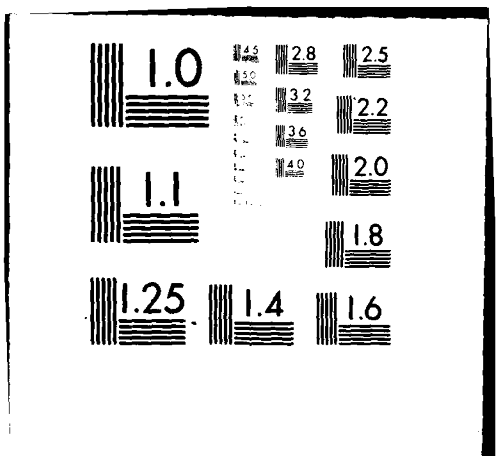

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RADC-TR-80-182
Final Technical Report
May 1980

AVAILABILITY/OPERATIONAL READINESS TEST SUBSYSTEM COST TRADEOFFS

Lockheed California Company

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This report describes the general test subsystem practices and tradeoff criteria that will make it possible for an equipment's or system's availability (or operational readiness) requirements to be met through the most cost effective usage of fault diagnosis/isolation/test subsystems that are used in conjunction with the maintenance of the equipment. The trade-off criteria are intended for use in planning the acquisition of new equipments and systems and to provide more accurate

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assessment of total life-cycle cost.

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EVALUATION

1. The objective of this study was to develop data and tradeoff information such that it would be possible for an equipment's or system's availability (or operational readiness) requirement to be met through the most cost effective usage of fault diagnosis/isolation/test subsystems and concepts.

2. The objectives have been satisfactorily fulfilled. The final report describes the basic design characteristics that impact the testability and resultant maintainability of the prime equipment and relationships between prime equipment design characteristics and the life cycle cost elements related to testability are derived. Advantages of Automatic Test Equipment (ATE) support over manually supported systems are discussed.

3. The tradeoff criteria developed in this study will provide inputs in planning the acquisition of new equipments and systems and help produce more accurate assessments of total life cycle costs.

JERRY F. LIPA
Project Engineer

EXECUTIVE SUMMARY

Compatibility between a prime electronic system and its support equipment has always been an important design requirement. With the increasing stress on system cost effectiveness and total life cycle system costs, the traditional, expedient, but costly approach to prime system/support system compatibility can no longer be tolerated. A more coordinated approach to electronic system design and support must be adopted. The time for initial consideration of a support system is during the conceptual design of the prime equipment. Only in this way can effective and practical trade-offs be made.

This report describes the basic design characteristics that impact the testability and resultant maintainability of the prime equipment. The relationships between prime equipment design characteristics and the life cycle cost elements related to testability are derived. The advantages of automatic test equipment (ATE) support are related to manually supported systems. The relationship of airborne and ground electronic systems is developed.

The tradeoff criteria developed are intended for use in planning the acquisition of new equipments and systems and to produce more accurate assessment of total life cycle costs.

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1. INTRODUCTION

1.1 Background

Compatibility between a prime electronic system and its support equipment has always been an important design requirement. Traditionally, the prime system and equipment designers have never felt constrained in their creative designs by possible limitations of the support concept or test subsystem. Generally, due both to scheduling problems and to a lack of appreciation for the effects of incompatibility, the prime-system design would progress to the point of design freeze before adequate emphasis was placed on the system support area. This independence of the prime system design threw additional burdens on the support system designer and often taxed his ingenuity beyond practical limits.

As long as support concepts were based largely on manual techniques, these compatibility problems did not require full solutions. Instead, field solutions had to be found by the support organization. Highly skilled maintenance technicians compensated for deficiencies and errors in maintenance documentation, invented ways of getting around test incompatibilities built into the prime system and equipment, and developed private failure libraries.

With the advent of automated support concepts, this compatibility area took on new importance. These concepts involved the use of military maintenance personnel with lower skill levels, who did not require comprehensive training regarding the prime systems.

With the increasing stress on system cost effectiveness and total life-cycle system costs, the traditional, expedient, but costly approach to prime system/support system compatibility can no longer be tolerated. A more coordinated approach to electronic system design and support must be adopted.

The time for initial consideration of a support system is during the conceptual design of the prime system. Only in this way can effective and practical trade-offs be made.

Preliminary maintenance and support concepts must be defined and optimized to reduce life-cycle costs. These include trade-offs involving the levels of built-in test and off-line test. Maintainability is defined as the probability that a device will remain operational or can be restored to operational condition within a specified period of time. Testability, one of the major disciplines which allows you to meet the maintainability goal, is defined as the inherent capability of a design to allow, as quickly as possible, the determination of operability and to provide the visibility to detect and isolate malfunctions.

The interaction between the engineering efforts of systems design, testability, and reliability, to name a few, is not easy to achieve. Testability will be a viable tool only if it is considered a design element and not a maintainability function. Attention to these interactions will lead to a reduction in the cost and complexity of test program sets, measured in simpler test interface devices, in software (for ATE systems) that is relatively easy to generate and has a minimum of execution time, and finally is easily adaptable for all levels of maintenance.

Figure 1 shows graphically that early expenditures to achieve better testability pay off in a lower cost of maintenance over the useful life of the equipment.

This report describes the general test subsystem practices and trade-off criteria that will make it possible for an equipment's or system's availability (or operational readiness) requirement to be met through the most cost effective usage of fault diagnosis/isolation/test subsystems that are used in conjunction with the maintenance of the equipment.

The trade-off criteria are intended for use in planning the acquisition of new equipments and systems and to provide more accurate assessment of total life-cycle costs.

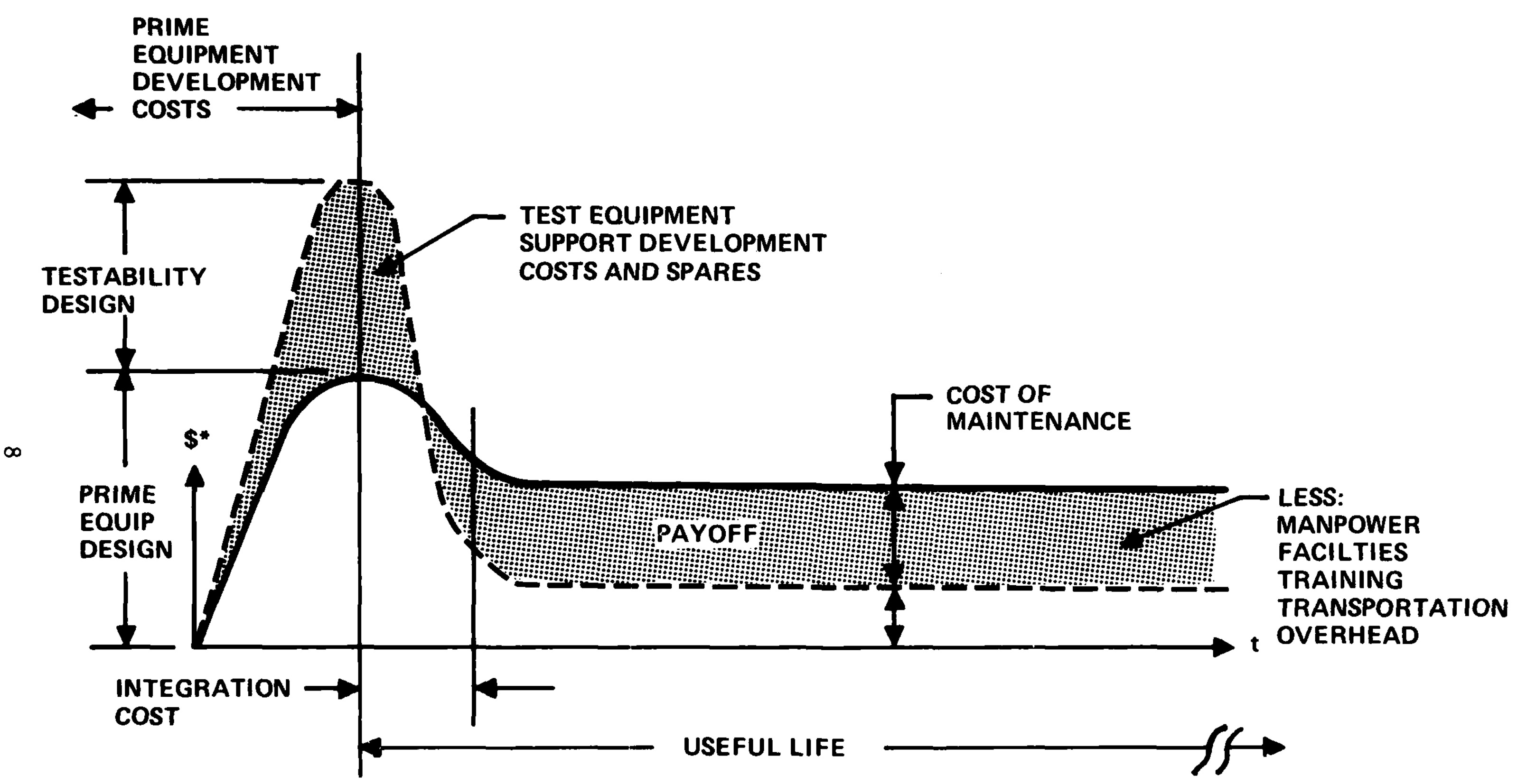

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Figure 1. - Testability impact on life cycle costs.

1.2 Availability/Operational Readiness

Availability and operational readiness are separate terms with the same objective. Availability for a continuously operating system is a classic reliability/maintainability term for expressing the predicted probability that the system is able to perform its mission.

$$A = \frac{MTBMA}{MTBMA + MTTR} \qquad (1)$$

where

A is prime equipment availability expressed as a probability (continuous operation).

MTBMA is the predicted mean-time-between maintenance actions.

MTTR is the predicted mean-time-to-repair (including fault detection/isolation).

Operational readiness (OR) is used to express the probability that the equipment is available to perform its mission. In the case of aircraft systems OR is computed as a function of aircraft available hours. For ground equipment OR is based on available operating time.

$$OR = \frac{\text{Ready Hours}}{\text{Total Hours}} \qquad (2)$$

where

Ready hours are equal to the total hours less nonready hours (NOR). NOR includes time lost due to a malfunction (including fault detection/isolation).

In reporting failures, the term MTBMA (Mean-time-between-maintenance-actions) is used to express the maintainability of the prime equipment and includes scheduled and unscheduled maintenance as well as retest okay conditions. MTBMA may be expressed in flight hours or equipment operating time, depending on the maintenance reporting system.

Figure 2 shows the relationships between availability/operational readiness and life cycle cost elements as a function of the maintainability of the prime equipment. By designing testability into the prime equipment the downtime can be minimized. The following sections describe these relationships.

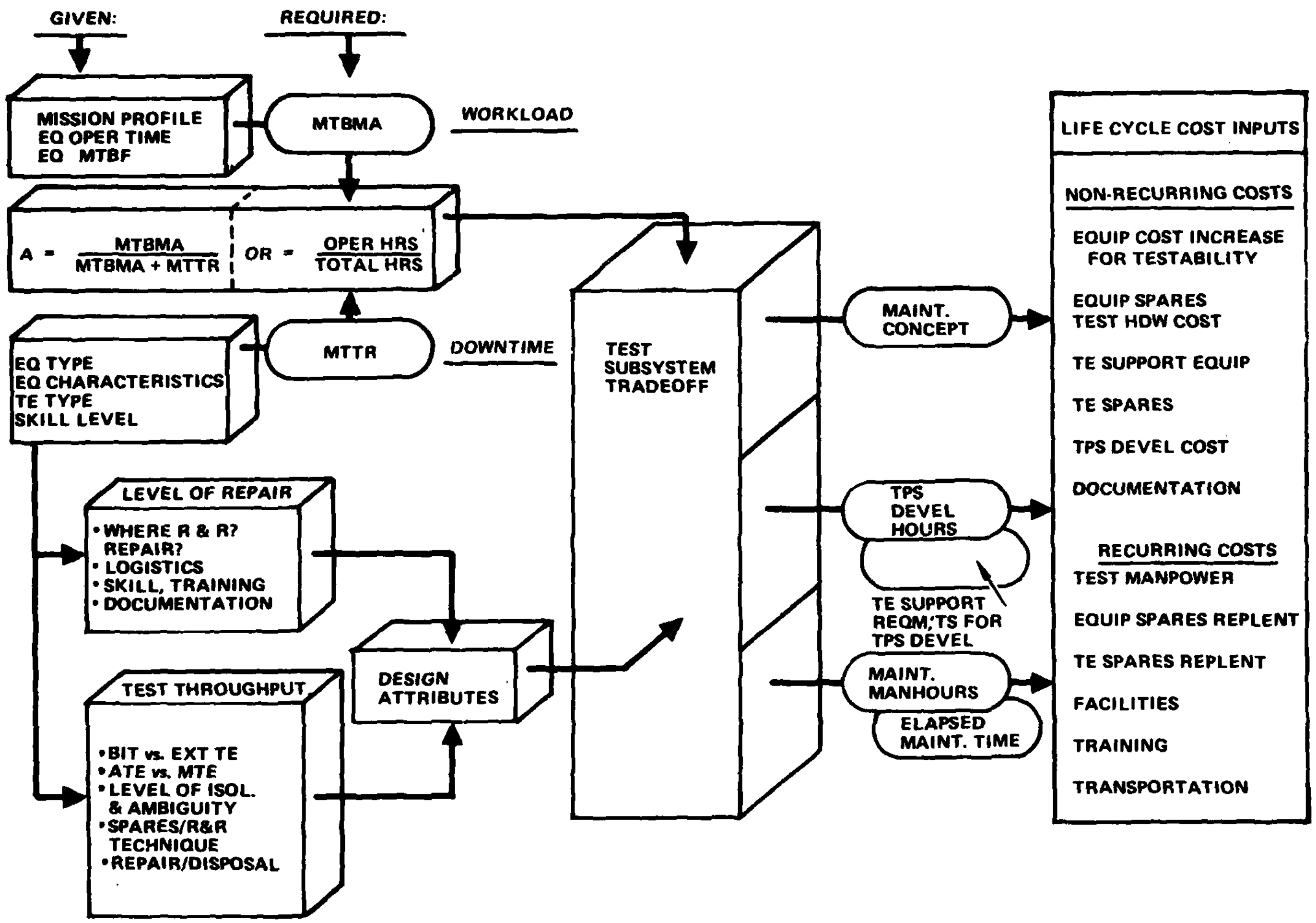


Figure 2. - Availability/operational readiness test subsystem cost trade-off relationships.

1.3 Test Subsystem Description

The test subsystem consists of all elements of the test equipment, prime equipment, test program, and support equipment required to maintain the prime equipment system. It is important to consider all elements in the development of a maintenance concept for a given system. The test subsystem includes:

(a) Unit Under Test (UUT). The prime equipment, which may include built in test (BIT) and test adaptable features.

(b) Test equipment external to the UUT.

(c) Test program set (TPS) or items of support equipment used in the testing of the UUT.

(d) Logistic support items which impact the cost of maintenance.

1.3.1 Unit Under Test (UUT)

The unit under test (UUT) is the prime equipment which requires maintenance support. This may be an entire system, a group of or single line replaceable unit (LRU) or "black box(es)", or a submodule called a shop replaceable unit (SRU). The equipment design must include testability as a prime consideration. The extent of testability features used will depend on the level of repair (LOR) required to achieve the maintainability goals. To achieve the testability goals, the following equipment design characteristics must be considered early in the development cycle:

- Mechanical design
- Functional modularity
- Tolerance considerations
- Test points
- Built in test (BIT)
- Test Operator Actions and Skill Level

1.3.1.1 Mechanical design. - Major assemblies are generally packaged in small, compact chassis, with a minimum number of surface connectors for input/output signals and with a few selected test points. For optimum testing, the rules for packaging and for bringing out UUT signals and test points to surface connectors are somewhat different. For example, the input/output interface must also facilitate performance testing and fault isolation of the assembly itself. This could mean more test points and associated wiring and connector terminals, more shielding; and larger connectors on both assemblies and subassemblies. The criteria for mechanical design also become more stringent in terms of human factors, particularly component accessibility and replacement, equipment handling, and cable hookup and disconnect. Independent test of associated assemblies and subassemblies is required. Packaging should also consider cooling temperatures of the UUT in the test environment.

Packaging of LRUs, SRUs, and sub-SRUs is an important factor in testability. High reliability can be obtained by decreasing the number of SRUs and sub-SRUs in a LRU particularly in relation to the number of connectors and the amount of interconnection wiring. Continuing advances in packing density within ICs should be a big advantage to electronic designers. Coupled with the use of microprocessor software and distributed processing, many hardware functions can be reduced or eliminated.

Since test interface hardware is designed as part of the test program effort, it is necessary during the prime hardware design to establish ground rules for the selection of connectors and for pin assignments. The use of standard connector types and uniform pin assignments facilitates the design of interface devices (IDs) to test large numbers of UUTs.

1.3.1.2 Functional modularity. - Current state-of-the-art electronic components are conducive to modularized packaging. This is particularly true in the case of integrated circuits. For test compatibility, modularization alone is not the sole design criterion. Circuits must be designed and packaged according to function to facilitate performance testing, fault isolation, and repair.

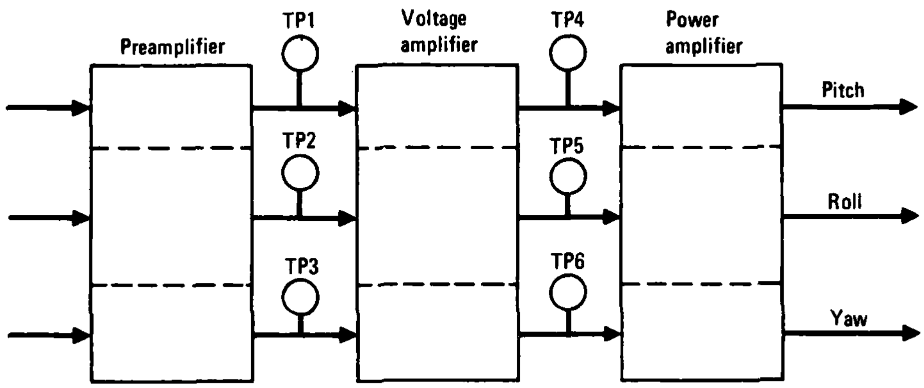
LRU's should contain functionally modularized SRUs that are easily removable. There is a direct relationship between functional modularity and fault isolation. As a rule, the higher the degree of functional modularity, the less time spent in fault isolation and repair. This is true for any electronic device whether it is tested manually or on automatic support equipment.

The major differences between functional and nonfunctional modularity are illustrated in Figure 3. The design in Figure 3A is packaged in such a way that the pitch, roll, and yaw signals are conditioned and amplified by three separate modules, namely, a preamplifier, a voltage amplifier, and a power amplifier. Each contains three independent identical channels, one for each different signal. If the performance level of a particular signal drops below a predetermined limit, then isolation to the faulty module is usually accomplished by measuring for specified values at appropriate test points, as shown. A major advantage of this design is that individual modules can be readily built and tested in quantity by the manufacturer, and can be improved in reliability and size as state-of-the-art progresses. One major disadvantage is that separate test points must be provided for each individual module for purposes of fault isolation.

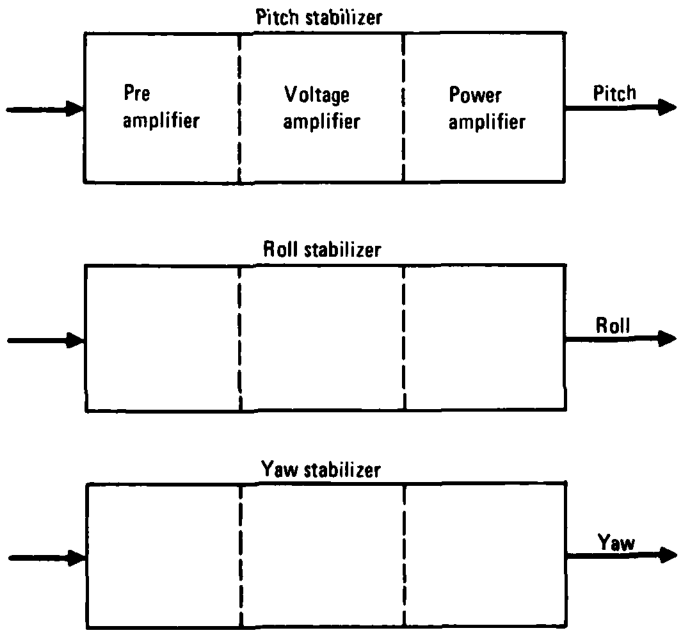
With the design in Figure 3B, each signal channel is packaged functionally, so that the associated preamplifier, voltage amplifier, and power amplifier are all mounted on the same module. In this case, no test points are necessary for fault isolation because each channel can be tested individually and unambiguous fault isolation can occur.

Illogical packaging can also result in excessive number of interconnections between modules. Figure 4 shows a classical example of excessive pins required by poor functional modularity.

1.3.1.3 Tolerance considerations. - The equipment designer must establish test tolerance values at all levels of test with tighter tolerances at the factory level, increasing as shown in the tolerance cone in Figure 5. This will preclude bouncing the UUT back and forth between levels of repair. If

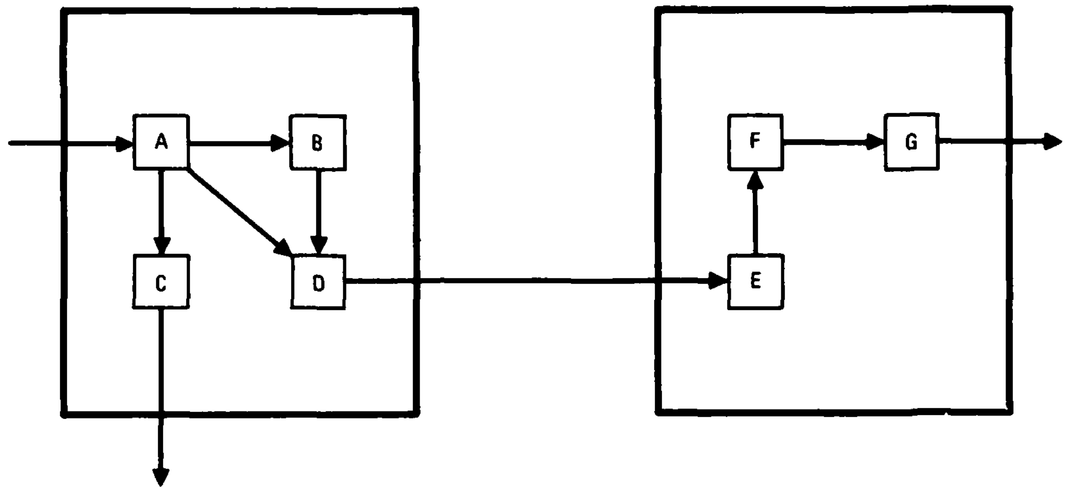


(A) Non functional packaging

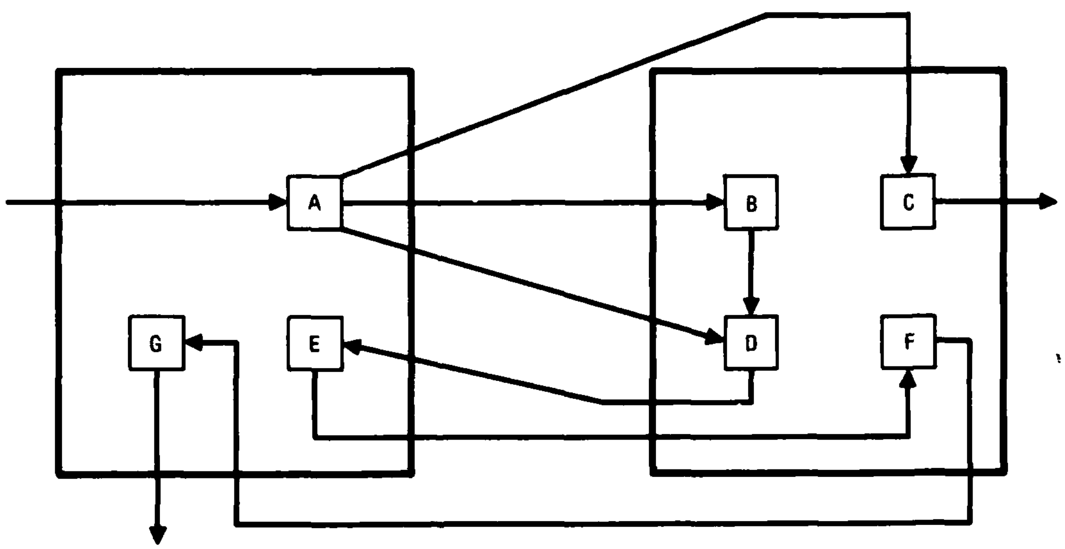


(B) Functional packaging

Figure 3. - Functional and nonfunctional packaging.



Correct
(Minimum interconnection)



Incorrect
(Excessive interconnection)

Figure 4. - Example of illogical packaging.

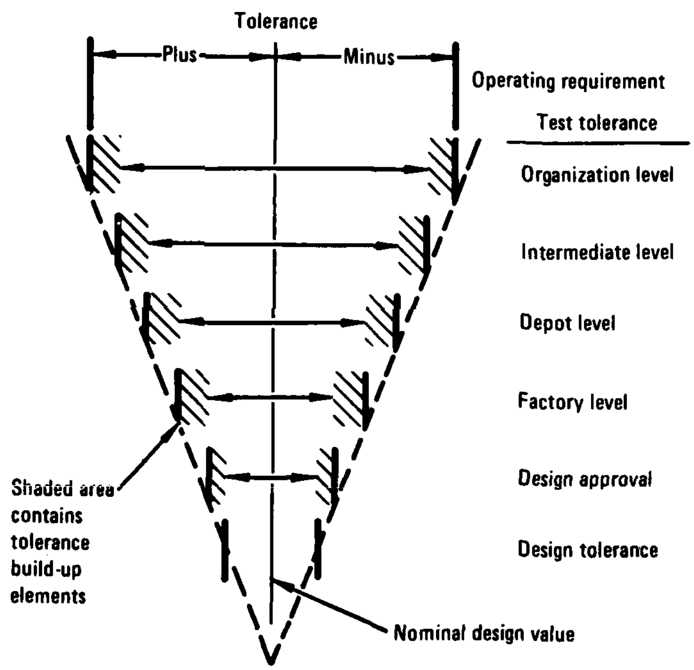


Figure 5. - Tolerance cone.

the designer does not consider the tolerance cone in development, tighter test requirements will result in organizational-level and intermediate-level overdesign and increased acquisition costs for the UUT.

1.3.1.4 Test points. - Sufficient test points must be provided at readily accessible areas to permit nonambiguous fault isolation. At the LRU level, test points should be provided on functional or separate connectors with proper isolation or buffering to eliminate loading the functional signal path. The design goal is to provide sufficient test points to isolate malfunctions to a single SRU using both functional and extra test points. At the SRU level, test points should be brought out to designated pins on the input/output (I/O) connector and, if sufficient pins are not available due to size or spare pin requirements, a separate connector on the SRU should be used to house the remaining test points. The minimum requirement at the SRU level is the use of discrete terminal posts for probing, but the use of scattered test points does not lend itself to efficient automatic testing. At the sub-SRU (SSRU) level, test points should be provided to isolate faults to the SSRU or the components on the parent SRU.

1.3.1.5 Built-in-test. - Built-in-test (BIT) includes any self test used for evaluating the performance of the UUT, either alone or in combination with other test equipment. BIT is primarily designed into the UUT to improve maintainability at the organizational level. Proper BIT design can also provide improved test capabilities at all levels of repair.

BIT is the subject of a separate study by Rome Air Development Center [1] and will not be discussed in detail in this report. A general summary of this study is depicted in figure 6 and described below:

- The addition of BIT to the LRU can lead to lower maintenance time/cost at a minimal decrease in equipment reliability.
- The typical range of BIT is 5 to 15 percent, depending on the equipment complexity. (Computed as a ratio of BIT to total component failure rate.)
- The percent of an equipment normally tested by BIT is in the range of 83 to 95 percent. (Computed as a ratio of BIT monitored to total equipment failure rate.)

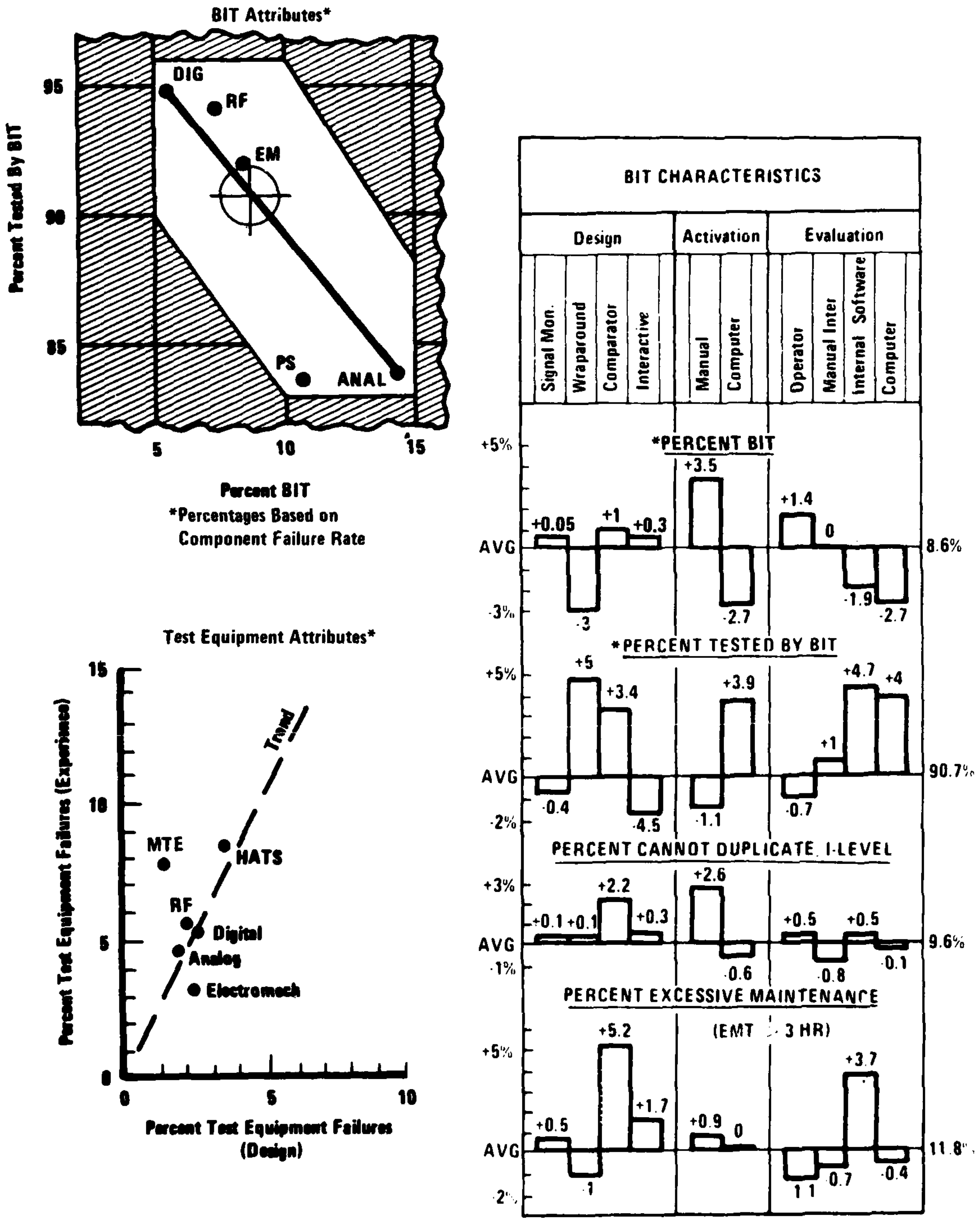


Figure 6. - Summary results BIT and TE characteristics.

- Type of BIT design results in different performance characteristics:
  Wraparound - Test signal routed through input and monitored at output.
  Signal Monitor - Test points monitored by level detectors.
  Comparator - Dual channel monitor with difference detected by BIT.
  Interactive - Monitors system and changes operation (e.g. shut down on failure) to backup system.
  BIT Activation - Manual (operator) or computer controlled.
  BIT Evaluation - Manual, computer, manual intervention, or internal software.
  The most effective BIT characteristics are:
  Design - Wraparound testing or signal monitoring over comparator and interactive BIT.
  Activation - Computer over manual.
  Evaluation - Dependent on weight of BIT design attributes and maintenance effectiveness. Operator evaluation is best from a least maintenance time standpoint and manual intervention in the case of cannot duplicate at intermediate level. BIT design attributes favor computer evaluation.

- Airborne and rack mounted (ground) electronics have the same effectiveness for a given percent BIT, when total maintenance time is considered.

- Design trade-off equations produced using multiple regression techniques provide a high level of correlation for predicting actual test equipment failures.

  Percent of failure rate tested by BIT:

$$\begin{aligned}\%\ \text{TSTBIT} = {} & 96.1 - 0.59(\text{No. of LRU per sys.}) + 0.00075(\text{No. of components}) \\ & + \text{Equip. type} \begin{bmatrix} -8.88 & \text{(Analog)} \\ 0 & \text{(Other types)} \end{bmatrix} \\ & + \text{BIT type} \begin{bmatrix} -4.2 & \text{(Sig. Mon.)} \\ 0 & \text{(Comparator or Wraparound)} \end{bmatrix} \end{aligned} \tag{3}$$

  Percent of failure rate of ext. TE to prime equipment:

$$\begin{aligned}\%\ \text{TEFAIL} = {} & 6.29 - 0.026\ (\text{weight, lbs}) + 0.0056\ (\text{power, watts}) \\ & - 0.37(\text{No. of LRU per sys.}) - 0.00014(\text{No. of components}) \\ & - 0.00016(\text{No. of failure modes}) \\ & + \text{Equip. type} \begin{bmatrix} -1.17 & \text{(Analog)} \\ -2.11 & \text{(Digital)} \\ 0 & \text{(RF, P.S. or Electromech)} \end{bmatrix} + \text{BIT TYPE} \begin{bmatrix} 0 & \text{(Comparator)} \\ -2.25 & \text{(Wraparound)} \\ -1.74 & \text{(Sig. Mon.)} \end{bmatrix} \\ & + \text{Activation} \begin{bmatrix} 0 & \text{(Manual)} \\ 0.77 & \text{(Computer)} \end{bmatrix} \end{aligned} \tag{4}$$

Average Elapsed Maintenance Time-Hours:

$$EMTO = 0.88 + 0.0062\ (\text{WEIGHT, lb}) - 0.00071\ (\text{Power, watts}) + 0.070\ (\text{No. of LRU per Sys}) - 0.0047\ (\text{No. of SRU per LRU}) + \text{Eq. type} \begin{bmatrix} 0 & (\text{Electromech, P.S.}) \\ 0.48 & (\text{Analog}) \\ 0.35 & (\text{Digital}) \\ 0.24 & (\text{RF}) \end{bmatrix} \quad (5)$$

1.3.1.6 Test operator actions and skill level. - Users of manual test equipment (MTE) are skilled technicians, thoroughly familiar with the UUT, who can be expected to apply considerable judgment and experience in troubleshooting UUT (and test equipment) failures. With ATE, however, troubleshooting procedures are embodied in the test program. The operator is usually less familiar with these procedures, as well as with the operation of the UUT itself. Therefore, one cannot depend on the ATE operator for correcting procedure errors, for interpreting results, or for fault isolation.

In automatic testing (ATE), the operator is the slowest element in the loop, and should be used for selecting a test program, connecting IDs and cables, and monitoring the test progress as annotated on the ATE display and in the instructions. Manual actions (alignment, adjustments, control settings, etc.) should be avoided. Alignment and other out-of-tolerance corrections should be performed in diagnostic loops which return the program to a GO path if successful. All manual operations should be clearly annotated in the instructions to avoid confusion.

The significant difference between automatic and manual testing is the application of the computational and logical capabilities of the ATE computer. Long, involved calculations, or complex logical sequences which would thoroughly confuse the average technician are now entirely feasible. Troubleshooting is not limited to simple step-by-step signal tracing. More sophisticated diagnostic techniques which use the capabilities of the ATE computer can be applied to achieve more reliable fault isolation with fewer test points.

1.3.2 Test Equipment

Test equipment (TE) used for supporting the UUT will depend on the level of repair (LOR) and the BIT used in the UUT. The choice of manual TE (MTE) or automatic TE (ATE) will be determined by trading-off the maintenance requirements and rate of inductions into the repair cycle. MTE is usually selected for low induction rate items or devices too simple to require ATE.

The use of external TE at the organizational level (O-Level) should be avoided. BIT will usually suffice in avionics, shipboard, and ground environments to avoid extra equipment or connections to isolate malfunctions to the LRU at O-Level.

At the intermediate level (I-Level), both MTE and ATE are used to minimize the logistic pipeline to the depot or factory repair facilities. All UUT testers consist of the same basic set of support equipment, but differ in characteristics depending on the type of TE and test skill level requirements. The support equipment required to implement testing of a UUT with a given tester is called the test program set (TPS).

1.3.2.1 Manual test equipment (MTE). - Manual test equipment (MTE) consists of a group of standard test equipment or an especially designed tester for a given UUT or system. The MTE provides stimulus and measurement devices to monitor the performance of the UUT. When a malfunction occurs, the test program instructions are used to deduce the functional area of the UUT in which SRU substitution or alignment is required. Printed circuit board extenders and probing are often employed to isolate faults. In using MTE, a great deal of latitude in operator judgment is required, thus requiring a greater knowledge of the UUT operation than is required for ATE. MTE supported test programs tend to have longer run times than an equivalent ATE due to operator actions.

1.3.2.2 Automatic test equipment (ATE). - Automatic test equipment (ATE) consists of a basic computer, stimulus/response devices, and an operator interface to control and observe testing of the UUT. The common media for test programs to control UUT testing are paper or magnetic tape and disc. Figure 7 shows a general block diagram of a typical ATE. The computer controls the stimulus, response, and power supply sections of the ATE. The stimulus/response signals from the ATE are routed through the input/output (I/O) section of the ATE to the interface device (ID), which is part of the UUT test program set (TPS). The design of the I/O varies for different ATE and is a major cost consideration of TPS design. Some ATE have stimulus/ response signals that are terminated in all dedicated pins at the interface; others have all universal switching. The use of universal switching can greatly reduce the cost of ID design by reducing complexity of the elements in the ID.

ATE is packaged in racks or consoles with layout for human factors being a prime consideration. Smaller ATE is sometimes used for operational level testing, usually in a portable "suitcase" but is not recommended. Built-in Test (BIT) is preferred in the flight line or the organizational level environment.

Built in test (BIT) is a special subset of ATE. BIT, is sometimes used in conjunction with ATE to enhance fault isolation capabilities at all levels of repair. The last category of ATE is the bench tester, especially designed for submodule testing at depot levels. Bench ATE is usually specialized for one type of module; for example, digital printed circuit cards.

The following description is the normal method of operation using the TPS of a typical ATE as shown in figure 7. The test program is prepared by the test design engineer during development. The test requirements specified in the Test Requirements Document (TRD) are converted to the test program language, such as ATLAS. The test program is then processed by a compiler into the machine code used by the ATE and stored on magnetic tape or disc, item (1). At run time, the test program is loaded into the ATE core memory and is executed in much the same way as any other computer program. The UUT is connected to the ATE via the ID, item (2). As the program is executed, one or more stimuli are selected and routed to the UUT.

Simultaneously, a response from the UUT is conditioned and measured by the response section of the ATE. Measured values can be stored for later evaluation or compared immediately against pre-established limits. The results of these evaluations and comparisons determine the sequence of tests which may lead to an all-Go indication or to identification of a faulty UUT subassembly or component. Test data and operator instructions are generally displayed during program execution on the CRT display. Other operator actions, such as setup, loading, adjustments, etc., are annotated in the test program instruction (TPI), item (3). Operator responses are entered via the operator interface (ATE keyboard) by positioning UUT controls, or by changing interface connections as instructed by the TPI. When testing is complete, the operator is instructed by the CRT and TPI to remove the UUT setup or to execute a maintenance action.

1.3.3 Test Program Set (TPS)

The test program set (TPS) consists of the elements required to connect the test setup to the UUT, adapt the UUT to the given tester and properly instruct the operator in the testing procedure required. TPSs normally consist of three items: the test program, the interface device (ID), and the test program instructions (TPI).

1.3.3.1 Test program. - The test program is a step-by-step sequence of the tests required for a given UUT. For ATE it is a tape or disc containing the coded sequence which, when executed by the ATE, will provide the test subsystem with a set of instructions sufficient to ascertain automatically the operational readiness condition of the UUT, and if faulty, to isolate the fault to the required level for maintenance action. For MTE the test program is a testing table showing the sequence of events required in the testing process.

Test programs provide the sequence of GO/NO-GO operations for checking UUT performance and for fault isolation. The prime requirements of a good test program are:

- the ability to determine whether the UUT meets performance specifications

- the ability to fault detect and fault isolate the UUT effectively in a minimal period of time

- minimal effort on the part of the operator to prepare the UUT for test and to run the actual test program

- minimal effort on the part of the operator or maintenance technician to follow instructions for making adjustments, alignments, or repairs specified by the test program.

The effectiveness of any test program in accomplishing these objectives lies in the ability of the test program designer to fully understand the technology of the TE system, the UUT, and any engineering subtleties inherent in its design. A complete description of the test programming process, from initial design to validation, is provided in the test requirements documentation (TRD).

1.3.3.2 Interface device (ID). - The interface device includes hardware and/or cables to adapt the UUT to the tester. In the case of MTE, special cables are required to mate UUT connectors to the MTE. In the case of ATE an interface box usually terminates ATE to the UUT connectors. If incompatibilities exist in the I/O signals, special circuits are included in the ID to adapt the UUT to the TE. The degree with which compatibility is attained between the UUT hardware and the TE impacts the complexity of the ID and (in the case of ATE) test software. When testability is designed into the hardware, it can significantly reduce these costs. The effectiveness of TE support is directly related to the quality of the TPS and the design of the electronics.

1.3.3.3 Test program instructions (TPI). - The test program instruction (TPI) provides sequential directives for setup/teardown and execution of a test program, directs the operator and provides supplementary information needed for testing and on-line maintenance actions. Coordination of the test requirements documentation (TRD) with the data required for the TPI will save duplicate efforts in program preparation.

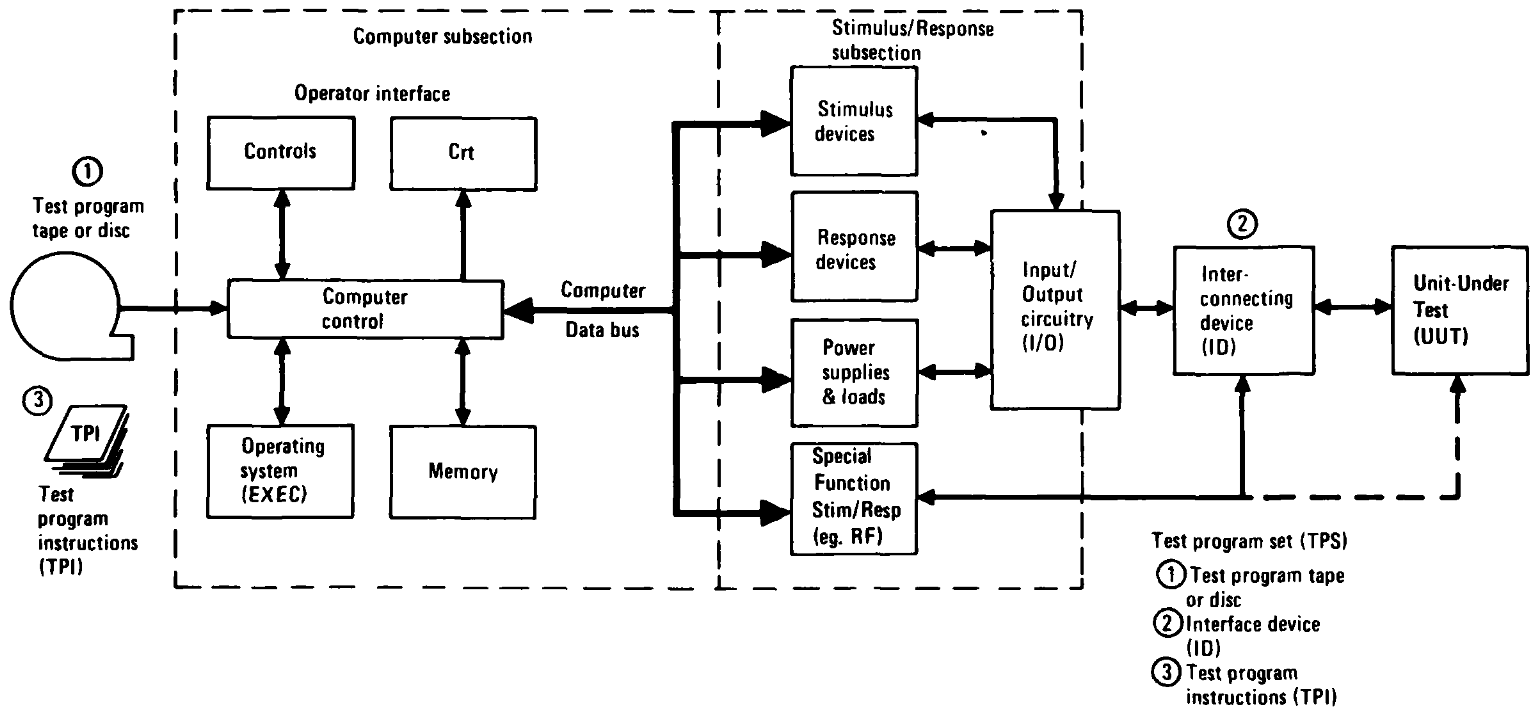


Figure 7. Simplified block diagram - ATE test subsystem.

1.3.4 Logistics Support

The selection of optimum combinations of logistic support must be considered in the development of the maintenance concept for the UUT. ATE presents a new set of problems not considered in MTE which must be addressed early in the development cycle.

The following list of items is an example:

- ATE/UUT test run time and operator action time.
- Unit modularity and testability.
- On-line module substitution and available spares.
- Operator skill level and maintenance instruction.
- Repair facilities and capabilities.
- Shop workload.

Life cycle costs (LCC) derived for a given UUT or system will determine the compliment of these factors required for a given test subsystem. This study will address some of the maintenance considerations which contribute to the LCC for a UUT. The manpower to support the maintenance of the UUT, the documentation and skill level of the test operators, spares requirements, tester maintenance, facilities, and transportation are all affected by the testability of the UUT and the level of repair required.

1.4 Maintenance Cycle

The maintenance cycle starts with the equipment failure, which is a function of the operating time and type of scheduled maintenance. Unscheduled maintenance is initiated at the organizational level (O-Level) and continues through the levels of repair until the UUT is again ready for issue (RFI) at the initial point of failure. This section will give a brief description of the maintenance cycle and the factors of design and logistics which impact life cycle costs (LCC).

Level of maintenance is dictated by the mission profile of the equipment (based on the operating time and environment). More reliable units will require less front-line spares and testing. All levels of test will require adequate attention to testability to keep the cost of support equipment and manpower to a minimum. The following maintenance considerations result in testability requirements for a given system:

- Level of repair
- Dispose-or-repair philosophy
- Level of fault isolation

1.4.1 Level of Repair

When a malfunction occurs, the test subsystem must be able to identify the area of the equipment which contains the fault so that with removal and replacement (R&R) procedures, the failed UUT can be ready for issue (RFI) with a minimum of downtime. The design characteristics of the UUT will determine the feasibility of repair at the three basic levels:

- Organizational level (O-Level)
- Intermediate level (I-Level)
- Depot level

1.4.1.1 Organizational level. - At the organizational level (O-Level) higher availability will be achieved by expedited fault isolation and modular replacement using built in test (BIT). The amount and reliability of BIT to meet the O-Level mean time to repair (MTTR) is a major design element in the development of the prime equipment. The accuracy and complexity of BIT will determine the amount of R&R (removal and replacement) that is feasible at O-Level and the need or elimination of the Intermediate Level testing for a given UUT. Figure 8 shows the general test flow of line replaceable units (LRU) through O-Level.

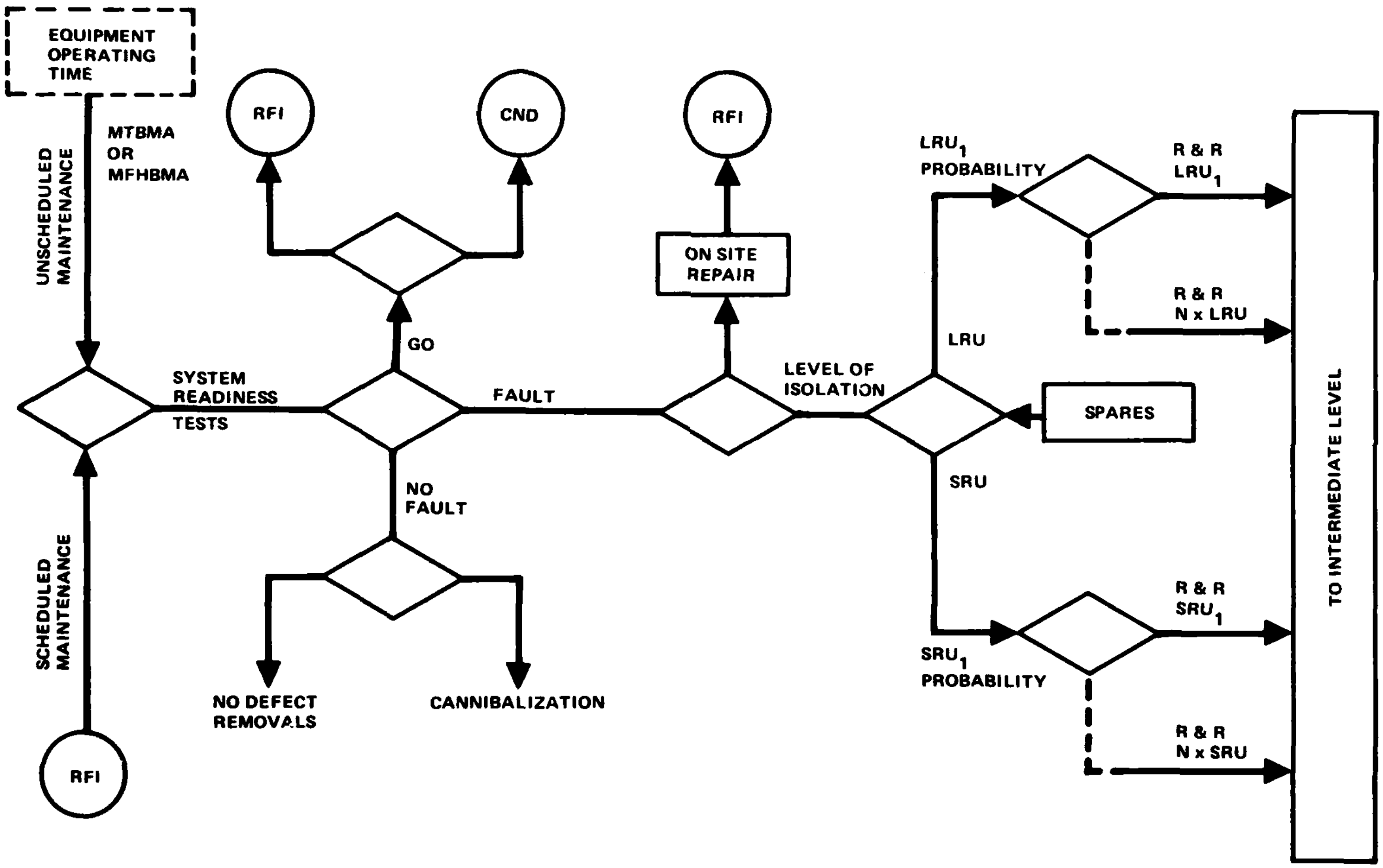


Figure 8. - Level of repair maintenance cycle - organizational level.

The importance of spares and rapid removal and replacement (R&R) can be seen in this diagram. The ability of the test subsystem to diagnose the malfunction accurately will reduce downtime. The level of isolation is also important in maintainability to prevent unnecessary removals and inductions at I-Level. The use of BIT reduces the maintenance personnel skill level required for testing.

1.4.1.2 Intermediate level. - LRUs which have been removed from the O-Level must be tested at either the intermediate level (I-Level) maintenance shop or sent to the depot or remote shop. Figure 9 shows the general test flow for the LRUs and shop replaceable units (SRUs) at I-Level. Experience has shown that the use of general purpose test equipment at I-Level and depot will reduce the cost of support equipment over specialized test equipment by high quantity purchase savings and less operator training. When very complex LRUs are tested at I-Level, long test times should be avoided by better testability design and BIT.

The maintenance reporting system reflects the total time to effect repairs, including problems in setup, spares availability, queuing, etc. Improved testability in equipment design characteristics can result in lower throughput or elapsed maintenance time (EMT). The ability of the test subsystem to fault isolate to a single module is a prime consideration in reducing EMT. Lower EMT reduces the number of testers and maintenance manhours (MMH) required at a given site. A small reduction in EMT and MMH yields a large cost savings in maintenance, thus the investment in more test program set development time (TPSHRS) is warranted to reduce total life cycle costs.

The most basic and critical decisions are those involving discard, repair, and levels of repair. These decisions control the development of initial maintenance support programs and impact dollars that must be spent in buying support. The impact of the repair/discard decision on the total maintenance support program makes it imperative that these decisions be made as an integral part of the equipment design.

A general rule (MIL-STD-2084) for determining repair or throwaway is to design the SRU or its submodules (SSRUs) for a cost-MTBF ratio of 0.01 dollar/hour or less.

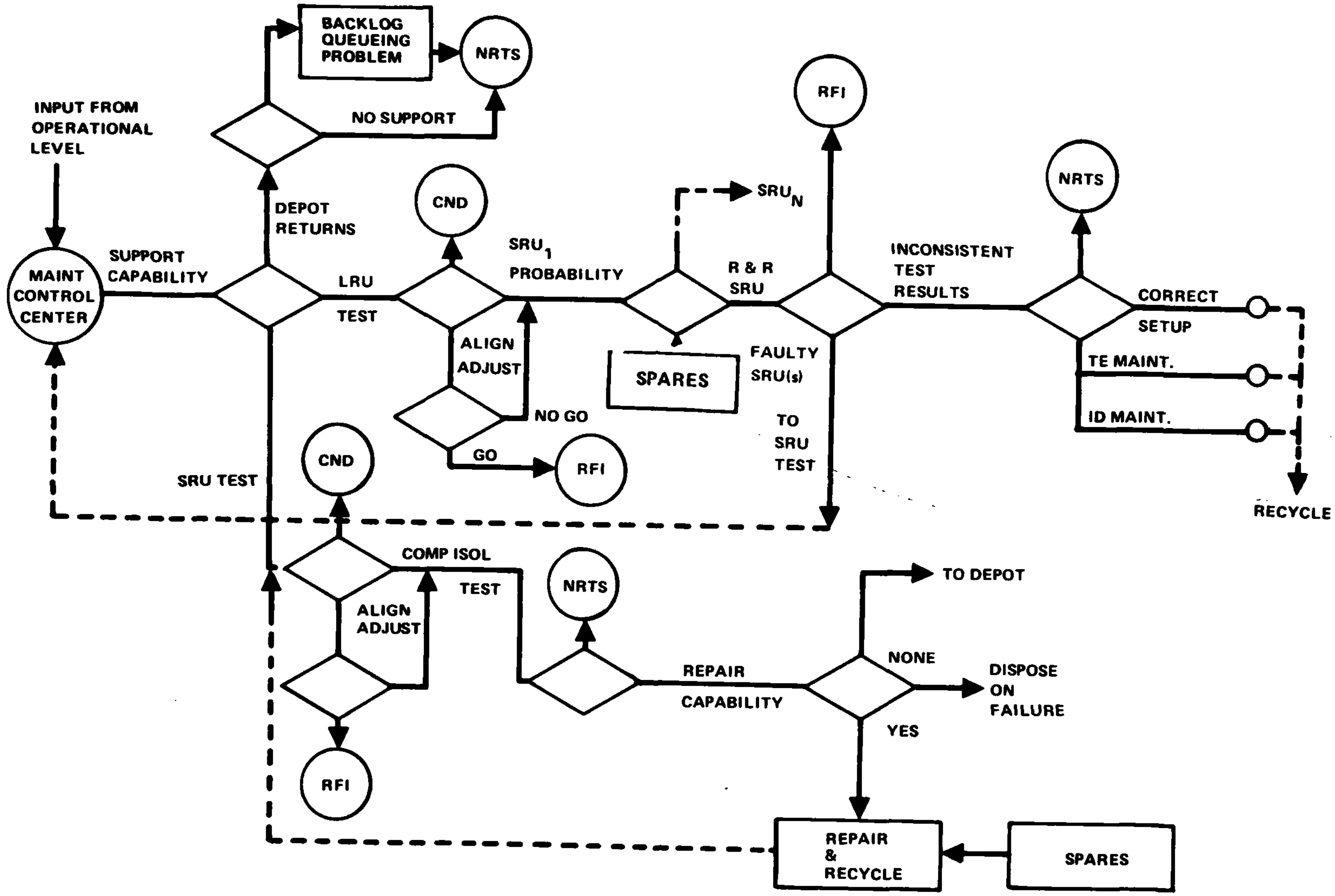


Figure 9. - Level of repair maintenance cycle - intermediate level.

1.4.1.3 Depot level. - LRUs and SRUs which cannot be repaired at I-Level are sent to the depot. This would include units with lower failure rates which do not warrant test support at higher levels. Depot level testing can include environmental factors which are not considered practical to test at I-Level. On the other hand, there is a strong tendency to send more UUTs to the depot than is cost effective when the extremely high cost of the logistic pipeline is considered.

1.4.2 BIT Versus External Test Equipment

The decision to use BIT in lieu of external test equipment should consider EMT and logistics. Using external test equipment at the organizational level, usually results in much higher EMT and the need for additional equipment and personnel to perform the test. At intermediate level, the use of BIT and external test equipment can reduce the total MMH to achieve a ready for issue (RFI) condition.

1.4.3 Manual Versus Automatic Test Equipment

Testability will improve test efficiency for both manual test equipment (MTE) and automatic test equipment (ATE). The need is more critical with ATE in order to benefit from the advantages of better throughput and lower skill level requirements. ATE should not be selected in situations where the cost of software development is not warranted, e.g., off-line continuity checks with a volt-ohmmeter for component isolation. Low failure UUTs would be candidates for general purpose MTE in the field, but may use ATE at the depot level.

1.4.4 Level of Fault Isolation

There are two levels of fault testing in the UUT. They are commonly referred to as fault detection and fault isolation tests.

Fault detection tests are also called performance, end-to-end, or GO-chain tests. It generally means a short, precise check to a very high degree of probability that the UUT is operational and performing its intended functions when installed in the next higher assembly. It does not mean that every stage or piece part in the UUT must be 100 percent perfect; rather, it must confirm the operational readiness of the unit for its intended mission.

Fault isolation tests are also called diagnostic fault isolation, fault isolation, or NO-GO chain tests. This generally means a short precise series of tests from a NO-GO branch of the performance (GO-chain) test for identifying, locating, and replacing a faulty subassembly or component. The capability of a semi-skilled operator or maintenance technician to locate and replace or repair a faulty item also enhances system maintainability and cost effectiveness.

The U.S. Navy documentation for defining sufficient level of repair in a test program is specified in MIL-STD-2084 (AS) (6). This document defines the probability of isolation to one, two, or three SRUs for LRU testing and four, eight, or ten components for SRU testing.

$$\text{Shop Non-Ambiguity Ratio (LRU Testing)} = \frac{\text{Number of SRU's isolated directly without ambiguity}}{\text{Total number of SRU's in the LRU}}$$

The minimum acceptable requirements for nonambiguous LRU fault isolation are:

a) In at least 90 percent of the cases of probable malfunction of a LRU, the fault should be isolated to that sole SRU.

b) In 95 percent, or more, of the cases of probable malfunction of an LRU, the fault should be isolated to that SRU and no more than one other SRU.

c) In all cases of probable malfunction of an LRU, the fault should be isolated to that SRU and no more than two other SRU's.

To quantify the LRU design ambiguity (AMBDES) in practical terms, the number of repair actions included in the test program is determined from the test requirement document (TRD) test flow diagram. The number of repair actions containing one, two, and three SRU decisions is calculated as a percent of the total number of repair decisions. The percent of single SRU decisions was used in this study as a measure of fault isolation quality. The actual LRU ambiguity (AMBACT) was computed from the data base results.

If the next lower level of the SRU is a sub SRU (SSRU), the ambiguity which is permitted in the automatic fault isolation process is the same as that specified previously under LRU shop nonambiguity ratio, except that the word "SSRU" is substituted for "SRU." If the next lower level of assembly contains discrete components (microelectronic integrated circuits, resistors, transistors, diodes, capacitors, etc.), the ambiguity which is permitted in the automatic fault isolation process is specified in MIL-STD-2084 under Shop Repair Test Points as follows:

- When the SRU contains 10 or fewer nonrepairables, isolation of groups of four or less should be possible for 50 percent of the possible faults. Isolation to four or less must be possible for all possible faults.
- When the SRU contains more than 10 nonrepairables, isolation to groups of four or less should be possible for 80 percent of the possible faults. Isolation to groups of eight or less must be possible for 95 percent of the possible faults. Isolation to groups of 10 or less must be possible for all possible faults.

The practical approach is to prepare a component check list. A SSRU is equivalent to one component for this analysis. During analysis, the number of remove and replace (R&R) decisions from the diagnostic flow chart (DFC) messages is annotated with the component check list. The shop non-ambiguity ratios shown above can be computed as a percent of the number of R&R messages.

SSRUs should be designed as "disposal-on-failure" items. As defined in MIL-STD-2084, a module with a cost-MTBF ratio of 0.01 dollar/hour or less should be designed for disposal-on-failure.

1.4.5 Removal and Replacement Techniques

The removal and replacement (R&R) of SRUs must be rapid to ensure low MTTR. The mechanical design should consider quick disassembly as a prime element. Spare SRUs should be stored near the tester to reduce logistics time. Some facilities use golden arm, or known-good modules for establishing a high confidence in the R&R decision while the LRU is still connected to the test setup.

1.4.6 Spare Provisioning

The provisioning of spares should be scheduled in a timely manner to take advantage of quantity purchasing of spare parts during the production cycle of the prime equipment. Sparing should be based on the predicted failure rate of the LRUs and SRUs as replaceable assemblies and not of their individual components. The sparing of components should be determined by the level of repair decision at intermediate, depot or supplier facilities.

At the organizational level, the number of spare LRUs should exceed the predicted equipment failure rate less the maintenance cycle repair rate. The number of spare LRUs can be minimized by adequate SRU spares at the intermediate or depot level.

At the intermediate level the number of spare SRUs should exceed the following expression:

No. of Spares =

$$\frac{\text{Oper. time/failure rate X Elapsed time/mission}}{\text{Turnaround time of logistics pipeline}} \text{ Minus I-Level Repair Rate}$$

The turnaround time of the pipeline can be reduced by improving the throughput rate of I-Level testing.

1.4.7 Repair Capability

A repair capability is essential at all levels. The extent will depend on the prime equipment maintenance concept selected. Operator training must include some O-Level repair activity to reduce turnaround time for minor failures, such as cables, buses, and antenna malfunctions. The I-Level should have printed circuit board repair capability as well as adequate training in isolating chassis faults and other minor procedures. Adequate attention to repair facilities can reduce setup/tear down time for maintenance actions.

1.4.8 Test Equipment Maintenance

The same attention in design for testability must be given to the test equipment as the prime equipment it supports. In the case of ATE, self test is mandatory with a minimum of external support equipment. A test program should have a preliminary confidence test of the tester and ID before initiation of the fault detection test. Complex test subsystem should incorporate wraparound tests to eliminate lost time which will occur if test setup or ATE failures are not detected in advance.

1.4.9 Manpower

The complexity of the UUT, the type of tester, and the level of test, impact manpower requirements. The use of BIT at the organizational level would tend to reduce manpower requirements. At the intermediate level, additional personnel are required for repair, tester maintenance, inventory control, administration, etc. By reducing the elapsed maintenance time, the maintenance manhours are reduced. These few examples show that improved testability reduces manpower requirements.

1.5 Life Cycle Cost Elements

The preceding sections have outlined the major elements of life cycle cost (LCC) which are impacted by the design of the test subsystem. By investing in additional nonrecurring costs in the early phase of development of new equipment, the recurring costs for its useful life can be reduced. This study develops trade-off criteria for evaluating the investment in terms of total LCC.

1.5.1 Nonrecurring Cost Items

1.5.1.1 Equipment cost increase. - The additions of BIT, test points, and other testability features will increase the initial cost of the basic prime equipment. The recurring cost of producing the equipment after development should be minimal. The Rome Air Development Center Built-In-Test (BIT) and External Tester Reliability study report (1) shows the relationships of BIT design to test performance. These relationships must be weighed against the mission requirements, operating time and equipment MTBMA to balance workload with downtime to achieve the required availability.

$$A = \frac{MTBMA}{MTBMA + MTTR} \tag{6}$$

The type of equipment will contribute to this decision, along with the skill level of the maintenance crew. This trade-off will determine the feasibility of O-Level support using BIT or I-Level or Depot support with MTE or ATE.

1.5.1.2 Equipment spares. - A well designed test subsystem will not achieve its testability goals, if inadequate spares are available to fill the logistic pipeline. Spare modules and submodules must be readily available at the point where the fault is detected to reduce MTTR. The spares requirement may be minimized by I-Level repair capability to offset the LRU and SRU failure rates.

1.5.1.3 Test equipment costs. - The selection of a tester to support the prime equipment must be compatible with the throughput requirements of the test subsystem and the skill level of the crew. A general rule would be to avoid special purpose test equipment (TE) and select general purpose ATE and MTE to satisfy workload constraints. If major incompatibilities exist in the TE interface with the UUT, special adapters can be used to eliminate the need for additional testers. The trade-off of tester compatibility with development cost of the data base is derived in section 3.1.1.1.

When the TE has been selected the LCC must consider the TE hardware cost, TE spares cost and TE support costs. The use of BIT in the prime equipment will offset a portion of the test support costs. BIT should also be a prime consideration in self test of the TE to eliminate additional TE support requirements.

1.5.1.4 Test program set development costs. - The development of test program sets (TPS) for the prime equipment is an initial nonrecurring cost which pays off in lower maintenance costs during the useful life of the prime equipment. TPS development costs must be considered for both ATE and MTE supported equipment.

Test Program Set development (TPSHRS) includes the following elements of cost:

	Element	Labor	Material
(1)	Acquire basic data on UUT for test analysis	In-house development or detailed review of vendor data	Outside purchase from vendor
(2)	Develop test strategy and document in the form of Diagnostic Flow Charts (DFC) and test setup diagrams compatible with tester to be used.	Perform test requirement analysis (TRA). Prepare test requirement document (TRD), including test interconnect diagram.	Digital stimulus/ response data may be purchased from vendor or produced using automatic test program generation techniques.
(3)	Interface hardware design and model	Document interface device (ID) hardware and build development model.	Hardware costs for raw material and electrical components.
(4)	Test Program Instructions (TPI)	Develop step-by-step procedure for on-station testing of UUT including operator actions to correct malfunctions detected.	Artwork costs and printing
(5)	Code/Compile (ATE) or Test Procedure (MTE)	Generate test program software using tester's higher order language (ATE) or prepare detailed test procedure (MTE).	Compiler operations and maintenance (ATE)
(6)	TPS Integration	Verification of test programs integrity by actual demonstration on station. a) UUT test performance debug b) UUT test diagnostic debug c) Fault simulation d) Test Program, ID, and TPI Updates	Repair facility support and tester maintenance

Element	Labor	Material
(7) Formal Sell-off (Validation)	Demonstration for inspection personnel and customer of TPS integrity. Includes functional testing and sample fault insertion.	Same as (4), (5), and (6)
(8) Verification	Demonstration of first production article on tester and fleet introduction.	Field service expenses

The complexity of TPS design will cause a wide variance in total manhours due to degree of testing required for the following reasons:

(1)	Level of Repair	Functional test with no diagnostics to full diagnostics.
(2)	Tester compatibility	Complexity of ID design to mate tester to UUT.
(3)	Test ambiguity	Degree of fault isolation to groups of SRUs, single SRUs or group of components.
(4)	Software update capability (ATE)	The flexibility of ATE software update from on-station patching (simple) to batch compilation on a separate computer (complex).
(5)	Verification and Validation (V&V) Requirements	Degree of sampling required to sell off TPS.

Data analyzed in this report include 64 LRUs from the S-3A system with full diagnostics, 90% test ambiguity to one SRU, batch compilation, 10% sampling for V&V and various degrees of tester compatibility. For this reason, test program set manhours (TPSHRS) has been normalized to provide a common scale for prediction of new acquisition costs.

$$TPSHRS = K_D * TPS \qquad (7)$$

where:

K_D is the complexity factor for a given UUT design characteristic. TPS is the manhours for basic TPS development of the simplest complexity. The simplest complexity is a unit with no fault diagnostic tests or active components in the UUT/tester interface. The data base used a batch compiler and 10% sampling for V&V.

The factors analyzed in this study are:

- Tester compatibility
- Functional modularity
- Type of electronics circuitry (discrete, integrated circuits, hybrid)
- Component density
- Level of fault isolation.

The equipment design characteristics which were evaluated to determine their impact on TPSHRS in this study were:

- Type of electronic equipment (digital, analog, etc.)
- Number of replaceable submodules
- Number of active pins in both LRU and SRU
- Number of active stages in the electronics
- Number of electronic components
- Number of failure modes.

1.5.1.5 Test station hours. - The number of test station hours used for development impacts the total life cycle cost. This includes setup time, test station maintenance time, idle time and useful TPS development time. If the number of hours exceeds the available schedule, more than one station will be required, including additional maintenance costs. Station hours (STAHRS) will be influenced by the following factors:

(1)	Level of Repair	Functional tests only to full diagnostic testing.
(2)	ID Complexity	Station time required to checkout ID, simple to complex.
(3)	Tester Software Update Capability	If tester has on-station software update capability, more station time is required than on off-station compiler.
(4)	Validation and Verification (V&V) Requirements	The degree of on-station time required to sell-off and verify TPS.

1.5.1.6 Test design documentation. - One of the major contributing factors to the high cost of test software development is the inconsistency in test documentation. New acquisitions should specify the test requirement documentation which will enforce the visibility in testability required for cost effective development of the maintenance concept for a given system over the entire life of the system. It should include top level test strategy and UUT descriptions and detailed test flow diagrams. Calculations of fault isolation capabilities will be included. Proper test design documentation will reduce the test documentation at other levels of development. For example, test design figures should be used for the test program instructions (TPI) which accompany the test program. TRD requirements are included in MIL-STD-2076 (AS) [4].

1.5.2 Recurring Cost Items

1.5.2.1 Maintenance manhours. - When more sophisticated ATE software is developed lower maintenance manhours per action at both operational and intermediate levels of test is expected. The following relationships were analyzed from the S-3A data sample to determine the degree of improvement.

$$MMH = MMHO + MMHI \tag{8}$$

where:

> MMH is total average manhours per maintenance action. MMHO and MMHI are average manhours per maintenance action at the organizational and intermediate level respectively.

MMH includes maintenance personnel required for the life of the system and includes overhead and material required at the test facility. MMHO is impacted by the degree of self-test the UUT or system contains and the accessibility of LRU for removal and replacement (R&R), MMHI is impacted by the type and complexity of the tester interconnection device (ID). The UUT complexity and SRU accessibility affect the time required to R&R modules during test.

1.5.2.2 Elapsed maintenance time. - The average elapsed maintenance time (EMT) is indicative of throughput for the maintenance action. Mean-Time-To-Repair (MTTR) is the same as EMT. Determination of EMT is required to plan for the number of test stations and maintenance crews required at each site. EMT is dictated by the mission requirements and priorities.

$$EMT = EMTO + EMTI \tag{9}$$

where:

EMT is the average elapsed time per action from test start to ready for issue (RFI) condition for both EMTO and EMTI.

EMTO and EMTI are organizational and intermediate test averages, respectively.

2. TECHNICAL APPROACH

The test subsystem elements described in section 1 were evaluated to determine relationships of testability characteristics on existing weapons systems. An in-depth study was accomplished on the S-3A Viking data, since most of the data were available for 64 test program sets developed for ATE testing and experienced field maintenance data were available. After this analysis was complete, the results were compared to the following systems:

S-3A Viking - 64 LRU's with BIT and which are supported by ATE.
- 17 LRU's which are supported by MTE.

C-5A Galaxy - 23 LRU's which use the MADARS on-board test subsystem as BIT. The intermediate support of the 23 LRU's was studied for 12 LRU's using ATE and 11 LRU's using MTE.

P-3C Orion - 13 LRU's were studied which are supported on-board by BIT and use MTE for depot support.

MK-86 Radar - 12 racks of ship-board electronics were studied which use BIT for testing and general purpose MTE for SRU replacement at the organizational level.

The study was limited to the analysis of those life cycle cost (LCC) elements which were experienced on the data sample that impact the intermediate level (I-Level) TPS development costs and the maintenance man-hours per action; and the average maintenance time per action at all levels during the life of the maintenance cycle. Average maintenance time per action or Elapsed Maintenance Time (EMT) equals the Mean-Time-to-Repair (MTTR). The effect of EMT is analyzed in this study. EMT differs from maintenance manhours (MMH) by the number of personnel involved directly and indirectly with the maintenance process.

2.1 Data Correlation Procedure

The analysis of the prime equipment attributes versus the resultant life cycle cost (LCC) elements was developed in the following manner. A computer correlation technique was used. The statistical package for the social sciences (SPSS) [2] software was used to refine data for accurate correlation of design parameters. The analysis used the following limits for the correlation coefficients (R) and coefficients of determination (R^2):

Degree	Correlation Coefficient (R)	Coefficient of Determination (R^2)
Good	.800	.640
Fair	.700	.490
Poor	.500	.250

Since this technique identifies the best linear equation through the data points, the natural logarithms of failure modes and components were also plotted to obtain the highest correlation. For error analysis the highest correlation (x or LNx) was used in the alogrithm.

2.1.1 Linear Correlation Analysis

The SPSS data was analyzed to determine acceptable correlations. Those items exceeding coefficient of determination (R squared) value of 0.640 were considered acceptable. Those with lower correlation were subjected to multiple linear correlation.

2.1.2 Multiple Regression Analysis

The second phase of the correlation analysis involved utilizing a stepwise multiple regression. In the analysis for each dependent parameter, a set of predictor or independent parameters is established. The computer then selects the best predictor based on correlation coefficient and enters it in the analysis determining the y axis intercept and slope of the best fit line. The program then recalculates the correlation coefficients and selects the second best predictor from among the remaining variables calculating a new y axis intercept and slopes for the parameters entered. The process continues until either all the parameters are entered for a preset tolerance or a goodness of fit or F ratio is met and a tolerance index T which is the tolerance on the multiple correlation coefficient R is met. The values used in the analysis are F = 0.01 and T = 0.001. During the regression, standard error is checked to insure that the value continues to decrease. When the standard error increases, the coefficients of the regression at the previous step are used. Multiple regressions were used to predict preliminary and final performance using the independent parameters based on the type of data available during progressive iterations in the design process. In general during early design phases, only rough estimated characteristics are known such as weight, volume, numbers of SRUs in the system and power. As the design develops additional data on number of components, number of pins in the units and the number of active elements are developed. During final stages of the design, exact data are available including component breakdowns sufficient to calculate failure modes. These breakdowns were used in groups of regressions considering the available design attributes as the design progresses. The multiple regression approach significantly increased the degree of correlation for the resultant conclusions drawn for all types of systems investigated.

2.1.3 Averaging

When neither simple correlation or multiple linear regressions resulted in an R squared greater than 0.640, average data were computed. In the case of R squared values between 0.490 and 0.639 both multiple correlation and averages were compared to determine the most logical conclusion from the data.

2.2 Testability Elements

Figure 10 shows the relationship of the prime equipment characteristics and the resultant recurring and nonrecurring life cycle cost (LCC) elements. The study was limited to the correlation of equipment design elements to the TPS development costs and long-term maintenance manpower savings.

2.2.1 Prime Equipment Design Characteristics

The following prime equipment design characteristics are listed in order of their availability during the development of the UUT.

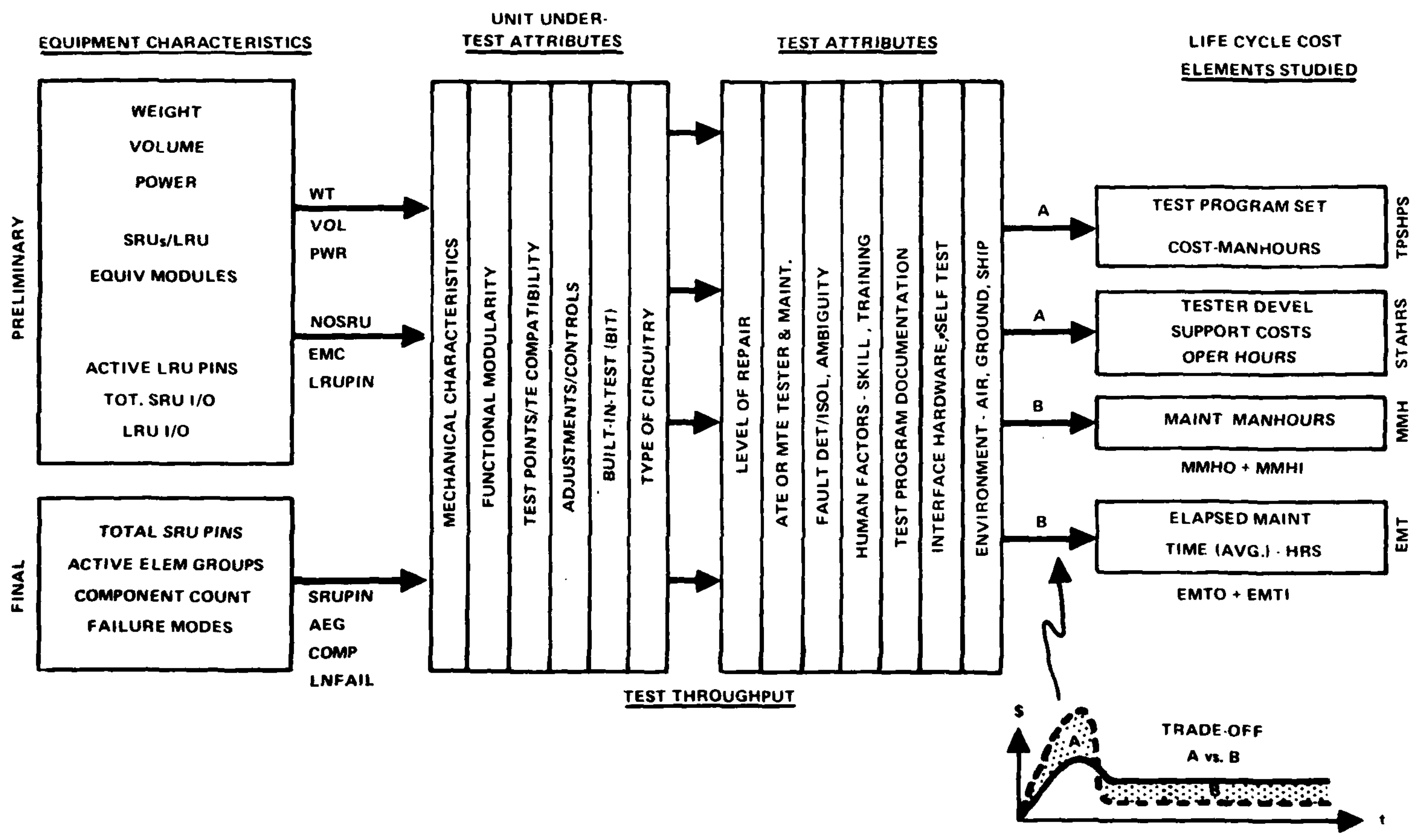


Figure 10. - Scope of trade-off study.

WEIGHT - LRU weight in pounds

VOLUME - LRU volume in cubic inches

POWER - Input power, in watts, to the LRU.

NOSRU - The number of SRU's in the LRU. The number of SRU's is not an accurate count, since there is a wide variation in packaging techniques. The equivalent module count (EMC) was used.

EMC - Equivalent Module Count is the number of replaceable units within the LRU with allowance for commonality and special features as shown below:

(a) Each unique SRU or SSRU, replaceable unit

(b) Parent SRU which mounts two or more SSRU's if it contains active components

(c) Chassis with major components other than connectors and mother board.

(d) Penalty count, add one for:

(1) Synchro/resolvers

(2) Data multiplex (e.g., Manchester I/O)

(3) Transducers

(4) Alignment or adjustments if greater than 5

(5) Drive mechanisms (e.g., tape transport)

(6) Special devices (e.g., microprocessors, optics)

(7) CRT/TTY/printers

(8) Operator controls/lights

0-4=0
5-10=1
10-20=2, etc.

(e) Discount for:

(1) Commonality, identical or similar SRA/SSRA

SRA/SSRA	EMC
2	2
3	2
4 or greater	3

(2) Regulator or power supply modules in LRUs, other than power supply units

Number	EMC
1-4	1
5 or greater	2

LRUPIN - The number of active pins at the LRU interface.

AEG - Active Element Groups. The number of transistors or tube stages, diode bridges and equivalent circuits within an integrated circuit.

COMP - The number of components in the LRU.

SRUPIN - The total number of active SRU pins within the LRU.

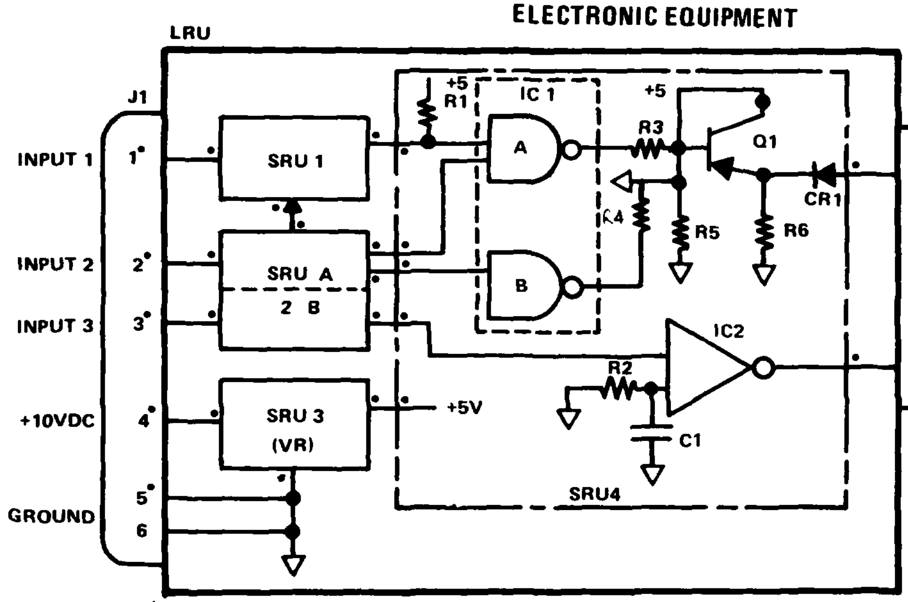
FAILMODE - The number of failure modes within the component count, computed as follows:

Component	Failure Modes
Resistor	1
Capacitors	2
Transistors	4
Diode - signal	2
Diode - power	3
Inductor - signal	1
Inductor - power	2
Integrated circuit	2 times inputs + 2 times outputs
Transformer	1 per winding
Relay	1 per pole
Filter	1
Switches	2

LNFAIL and LNCOMP - The natural logarithms of failure modes and components, respectively to improve linearity of correlation.

Figure 11 is an example of the process required to count the equipment elements.

ELECTRONIC EQUIPMENT



EXAMPLE COUNT:

NOSRU = 4
EMC = 5
SRUPIN = 17
LRUPIN = 7
AEG = 4 (SHOWN)
COMP = 11 (SHOWN)
FAIL MODE = 30 (SHOWN)
6R = 6
1C = 2
1Q = 4
1CR = 2
IC = 2
5 IN / 3 OUT } 8 x 2 = 16

LNFAIL = LN(30) = 3.4

AEG = ACTIVE ELEMENT GROUPS = TRANSISTORS, DIODE BRIDGES, EQUIV CKTS IN IC
EMC = NUMBER OF *FUNCTIONAL (TESTABLE) MODULES, CONSIDERING*
ADVANTAGES OF COMMON CIRCUITS AND PENALTIES OF
SPECIAL FEATURES:

RECT, REG 4 MAX	= 1
EXCESSIVE CHASSIS	+1
SYNCHRO/RESOLVER	+1
DATA MULTIPLEX	+1
1-5 ADJ/ALIGN	+1
DRIVE MECH	+1
CRT/TTY/PRINT	+1
TRANSDUCERS	+1
OPER CONTROLS 5-10	+1
10-20	+2
ETC	

COMMONALITY:

SIM SRUs #	COUNT
1	1
2	2
3	2
4	3
5	3

EQUIP. TYPE:
DIGITAL (BY % SRU 50%)
NON-DIGITAL
ANALOG
RF (freq)10 MHz)
POWER SUPPLIES, REGULATORS

Figure 11. - Equipment characteristics definition of elements.

2.2.2 UUT Test Attributes

The unit-under-test (UUT) design has other characteristics which impact testability as highlighted in section one. The following attributes of the UUT were examined against development costs and maintenance performance to identify those with the greatest effect on the life cycle cost (LCC) elements:

- Equipment type
- Packaging and electronic circuit type
- Percent built in test (BIT)
- Component density
- Functional modularity
- Tester compatibility

2.2.2.1 Equipment type. - Preliminary analysis of the data showed that digital test attributes were separate and unique from other types of equipment. For this reason, all data were evaluated as digital or nondigital. The definition of a digital LRU is one with over 50 percent of its SRUs with digital circuitry, excluding built-in power supplies or regulators. Digital equipment is normally duplicate channels of circuitry grouped in bytes. The exception is serial digital which contains unique channels. The complexity of the interface with the ATE must accommodate more active buffers in cases where the UUT is not compatible with the tester. On the other hand the debugging of digital software is simpler due to circuit similarity.

Nondigital equipment was evaluated in three subsets; analog, radio frequency (RF), and power supplies. Although the circuitry type and packaging requirements are quite different, the data showed a high similarity in test evaluation parameters. RF is defined as any LRU with frequencies exceeding 10 Megahertz. With frequencies over 10 Gigahertz, the complexity of the test interface increases thus having some of the same cost and performance results as digital circuitry.

2.2.2.2 Packaging and circuit type. - The type of packaging is not a major contributor to MTTR as long as the components are accessible, that is the SRU plugs into the LRU. The majority of the data base were discrete and integrated circuits mounted on printed circuit boards (PCB). RF components, such as microwave plumbing are treated as throwaway or return to depot items and have equivalent maintenance time as PCB replacement. The result of preliminary analysis showed that the mounting technique, provided it was modular, was not a major factor in test attributes. The circuit type included discrete components, cordwood discretes from the C-5A, and MSI integrated circuits. No LSI was available in this time period. The test attributes of circuit type were investigated in three categories:

- Discrete - greater than 75 percent discrete active circuits
- IC - greater than 75 percent integrated circuit active components
- HY - Hybrid of discrete and IC

2.2.2.3 Percent built in test. - The percent built in test (BIT) was computed as the ratio of predicted failure rates of BIT circuit components to the total number of components in the LRU. Data on 40 LRUs from the BIT Reliability study [1] were used with estimated ratios for the remaining LRUs. The relationship of BIT and EMTO was expected to correlate as a testability factor.

2.2.2.4 Component density. - The density of packaging components impacts the ease of repair. Since most of the maintenance data relates to remove and replace (R&R) time, the impact of component density was only a minor factor in accessibility. Evaluation was made by computing the number of components per cubic inch. High density was considered as greater than 3 components per cubic inch.

2.2.2.5 Functional modularity. - The impact of modularity is difficult to evaluate on a uniform basis. MIL-STD-2076(AS) [4] uses a grading system which includes the following categories for functional modularity:

(a) Each LRU function is contained within a single SRU and each SRU function is contained within a SSRU. (Good)

(b) The LRU is functionally modularized, but some SRU functions are not modularized within SSRUs. (Average)

(c) A few LRU functions are contained on more than one SRU, and/or most SRUs are not functionally modularized. (Fair)

(d) Most LRU function encompass more than one SRU. (Poor)

The method of evaluating a new system for modularity is time consuming and requires detailed data for accurate assessment. It would be done by examining the functional block diagram to determine the uniformity of signal flow from input to output without major loops. The functional description of the SRUs is a clue to good packaging. The presence of test points at each SRU is another indication of the potential for good fault isolation to a single SRU. The system used to evaluate the S-3A data was to assign a number from 5 (good) to 1 (bad) by grading the design ambiguity capabilities:

	DESIGN AMBIGUITY WEIGHTING POINTS		
% Ocurrances Isolated to:	>95%	>90%	>80%
1 SRU	3	2	1
2 SRU	2	1	0
3 SRU	1	0	0

Add points for 1, 2, and 3 SRU isolation. Assign a maximum of 5 and minimum of 1. This method of grading the resultant fault isolation ambiguity design was used in this study to simulate design evaluation.

2.2.2.6 Tester compatibility. - In this study, UUTs which had good tester compatibility (no active circuitry or major components) had approximately 10 percent of the cost of test program development for the ID. As the complexity of the UUT/tester interface increases, the ID design costs increase and the labor to develop and self test the ID increase. MIL-STD-2076(AS) [4] has three categories for evaluating tester compatibility:

- Stimulus and measurement accuracies
- Functional independence
- Power and load requirements

The ability of the tester to measure or generate a signal with an accuracy ten times the required UUT tolerance is considered good, with three times considered minimal. The need for adjacent circuitry to be build into the ID or buffering increases the complexity, but is done frequently to achieve compatibility with the assigned tester. The proper power, regulation and load requirements are essential to minimize ID complexity. These factors can be evaluated in the early development phase by comparing the UUT test requirements with the capabilities of the tester. Active circuitry, passive devices and the number of interface pins will determine the complexity of the ID and its impact on TPSHRS. The MMH and EMT have a minor increase due to automatic self test requirements in the case of a complex ID over simple ID.

In the S-3A data base, the number of active circuits, SRUs and components were evaluated to identify (1) simple, (2) nominal, and (3) complex IDs. In the general case, the number of components required for the ID (IDCOMP), the active circuitry (IDAEG) and the interface pin (LRUPIN) count would be computed:

IDVAL = IDAEG + IDCOMP/50 + LRUPIN/100

Simple, (1), IDVAL less than 10

Nominal (2), IDVAL value 10.1 to 100

Complex (3), IDVAL value greater than 100

As an example, a LRU with 10 active buffers (10 IC chips) and 10 load resistors for a 100 pin interface would have an IDVAL = 10 + 20/50 + 100/100 = 11.4, or a nominal ID complexity.

2.2.3 Other Test Attributes

Other test attributes that impact testability and resultant LCC are the use of ATE or MTE, the degree of the fault isolation requirements, and test environment.

2.2.3.1 Number of tests. - The number of tests required to isolate all components completely in a given UUT should be predictable from other UUT characteristics. It is difficult, if not impossible to predict the number of tests in the early phases of the development of a LRU. For this reason, the TPSHRS and STAHRS were evaluated by direct comparison with the UUT design characteristics. The run time of the test program was determined from design records for the S-3A data sample for comparison with EMTI. Run time is defined as the time to test a good UUT from the first test to the ready for issue (RFI) instruction. This ranges from a few minutes to over one hour in the case of complex LRUs. When setup time, fault detection, SRU replacement, and rerun time are considered the predicted run time should approach:

$$\text{RUNPRED} = 30 + 2\ \text{RUN} \tag{11}$$

where, 30 is the average data sample experience setup and teardown time.

RUN is the fault detection time with no faults. The reason for the 2 times RUN factor is to allow for the first fault detection run to the branch point for fault isolation (1/2 RUN), and another 1/2 RUN for the R&R time plus allowance for shorter runs when no fault is detected (CND case) and, finally, the rerun for final checkout (RUN). As a test program matures RUNPRED will converge with EMTI. RUNPRED is used as a measure of the testability of the UUT.

2.2.3.2 ATE versus MTE. - All systems in the data base use BIT as the major technique to isolate the first level of replaceable unit. For this reason, EMTO or MMHO should be relatively equal for the various systems. At the second level, some data result from the use of ATE and others from MTE. A direct comparison of percent difference in ATE versus MTE can be made for both EMTI or MMHI.

2.2.3.3 Fault isolation. - The level of fault isolation in the data base varies from a few cases of fault detection test only to full diagnostics. The design ambiguity (AMBDES) and actual ambiguity (AMBACT) were compared for the S-3A data base. There is a 2:1 ratio in the design to actual results due to the method of evaluating isolation. Future systems should weight the AMBDES percentage of isolation with the failure rate of the SRU in the test to achieve realistic predictability in maintenance time. In the data sample the cost of developing test programs with full diagnostics ranged from 25 to 75 percent of the TPSHRS. This attribute was examined by the degree of AMBDES versus TPSHRS, with higher percentages representing more complexity of isolation.

2.3 Data Sample

The following paragraphs describe the four systems used in the data base to evaluate testability elements. Table 1 shows a complete list of the systems and the extent of the evaluation performed. The selection was based on availability of development cost data and maintenance actions for the period of time shown below to determine realistic averages.

TABLE 1. - DATA BASE
EQUIPMENT INVESTIGATED FOR STUDY BY QUANTITY*

Item	S-3A LRUs		C-5A LRUs	P-3C LRUs	MK86 Racks
	ATE	MTE			
Type of Prime Equipment:					
Communications	8	1	3	3	12
Radar	4	8	3	2	
Navigation	10	2	8	2	
Computers	8	0	3	3	
Data Processing	21	5	10	4	
Mission Avionics	16	1	0	4	
Miscellaneous	8	5	0	0	
Modules:					
LRUs	64	17	23	13	12
SRUs	992	173	234	131	
Maintenance Concept:					
Organizational Level Testing	64	17	23	13	12
Intermediate Level Testing	64	17	23	N/A	N/A
Built-in-Test Capability	62		21		12
Modularity-Packaging	64		23	13	12
Skill Level Requirements	64		23		
Test Documentation	64		23		
Level of Isolation:					
O-Level to LRU	64	17	23	13	12
O-Level to SRU	N/A	N/A	N/A	13	12
I-Level to SRU	60		23	N/A	N/A
I-Level to Comp	500		234		
Life Cycle Cost Elements:					
Development Manhours	64				
Development Test Hours	64				
Maintenance Manhours	64	17	23	13	
Elapsed Maintenance Time	64	17	23	13	12
Test Equipment Used by LRU					
AN/USM-247 (VAST)	64	N/A	N/A	N/A	N/A
AN/USM-403 (HATS)	500	N/A	N/A	N/A	N/A
LORAL DATS	5	N/A	N/A	N/A	N/A
MADAR	N/A	N/A	23	N/A	N/A
Honeywell UG2395BA01	N/A	N/A	12	N/A	N/A

* Blank entries were not investigated in the study.

2.3.1 S-3A Data, ATE Supported

The S-3A Viking was evaluated to determine the trade-off criteria for the following testability life cycle cost elements:

TPSHRS - Test program set development costs (I-Level) in manhours.

STAHRS - Test program set development test station (I-Level) hours.

MMH - Maintenance manhours per action, based on a one year average (1977) at both O-Level and I-Level.

EMT - Elapsed maintenance time per action, based on a one year average (1977) at both O-Level and I-Level.

Table 2 identifies the 64 LRUs included in the data sample. Table 3 shows the equipment characteristics divided into digital and nonditigal categories. Table 4 shows the test attributes to be evaluated and Table 5 shows other test attributes evaluated in the study. Table 6 is the field experience for the 64 LRU supported on the AN/USM-247 Vestatile Avionics Shop Tester (VAST). The year 1977 was selected as a period after field deployment of the aircraft to eliminate early inefficiencies in training and logistics. The total flight hours for 1977 were 59,619.

Maintenance data were recorded in the U.S. Navy's Maintenance Material Management (3M) System.

2.3.2 S-3A Data, MTE Supported

Table 7 identifies the 17 LRUs surveyed from the S-3A which are supported by MTE at the intermediate level. These items were chosen to compare EMTI and MMHI with similar units from the ATE supported group. Table 8 shows the equipment characteristics and experience for the 1977 period of 59,619 flight hours.

Five of the selected LRUs were depot tested, thus no I-Level experience was obtained. The FLIR viewer had an extremely high maintenance time and was excluded from the computation of EMTI. The remaining 11 LRUs, supported at I-Level by MTE are compared to ATE supported LRUs in Section 3.2.3.

TABLE 2. - S-3A EQUIPMENT SAMPLE - ATE SUPPORTED

Function	System / LRU – Nomenclature	Type *	WUC	Acronym
Navigation	Airspeed Altitude Computer, CP1077/AYN5	DIG	5671100	AACS
	Flight Data Indicator Set, CD59/A			FDIS/
	Vertical Deviation Indicator, ID1780/A	AN	71B1100	VDI
	Horizontal Situation Indicator, 1D1779/A	AN	76B1200	HSI
	Navigation Data Repeater Converter, CV2854/A	DIG	71B1300	NDRC
	Doppler Radar Navigation Set, AN/APN200	RF	722F100	DOPPLER
	Inertial Navigation System, AN/ASA84 ( )	DIG	73B6100	CONT
	Navigation Control, C8746	DIG	73B6100	CONT
	Nav Data Converter, CV2745 ( )	DIG	73B6200	CONV
	Radar Altimeter Altitude Warning Set, AN/APN201 ( )			RAAWS/
	Radar Receiver Transmitter, RT1023 ( )	RF	722H100	RT
	RAAWS Height Indicator, ID1770 ( )	AN	722H200	IND
	Altitude Heading Reference Set, AN/ASN107			AHRS/
	Displacement Gyroscope, CN1366 ( )	AN	734M100	GYRO
	Analog-to-Digital Converter, CV2858 ( )	DIG	734M200	CONV
Communications	Communication Control Group, OK248 (V)/AI			CC/
	Intercommunication Station, LS801/AI	DIG	6435100	ICS
	ICS Communication Control, C8760/AI	DIG	6435300	IRC
	Switching Logic Unit, CV3043 ( )/AI	DIG	6435400	SLU
	High Freq Radio Set, AN/ARC153A			HF/
	Receiver Transmitter, RF1016	RF	6126100	RT
	Radio Frequency Amplifier, AM6384A	RF	6126200	PA
	Antenna Coupler, CU1985	RF	6126300	AC
	Ultra High Frequency Radio Set, AN/ARC156			UHF/
	UHF Receiver Transmitter, RT1017	RF	6327100	RT
	Data Terminal Set, A/D Converter, CV2830/AYC	DIG	69X2X00	DTS
Data Processing	General Purpose Digital Computer, AYK10 (V)			GPDC/
	Power Supply No. 1, PP6679 (P)	PS	73B1600	PS1
	Power Supply No. 2, PPS678	PS	73B1C00	PS2
	Power Supply, Computer Processor, PP6675	PS	73B1700	PS-CP
	Power Supply, Input/Output Sect., PP6677	PS	73B1800	PS-IO
	Power Supply, Memory Sect., PP6676	PS	73B1A00	PS-MEM
	Digital Magnetic Tape Unit, RD348/ASH	DIG	73X2H00	DMTU
	Tactical Acoustic Display Set, AN/ASA82			TDS/
	Tactical Acoustic Ind (Tacco & Senso), IP1054	AN	73B4300	TS
	Display Generator Unit, CV2806	DIG	73B4500	DGU
	Acoustic Readout Unit, IP1052	AN	73B4400	ARU
	Copilot Tactical Indicator, IP1053	AN	73B4200	C
	Pilot Tactical Indicator, IP1051	AN	73B4100	P

*DIG = Digital, AN = Analog, RF = Radio Freq., PS = Power Supply.

TABLE 2. - S-3A EQUIPMENT SAMPLE - ATE SUPPORTED (Continued)

Function	System / LRU – Nomenclature	Type *	WUC	Acronym
INCOS	Indicator and Armament Control Set, AN/ASQ147			INCOS/
	Armament Control Panel, C8857 ( )	DIG	73H2100	ACP
	Bomb Bay Command Sig Decoder, KY746	DIG	73H2300	BBD
	Bomb Bay Distribution Box, J3069	AN	73H2700	BBDB
	Copilot Indicator Control, C8859 ( )	DIG		C
	Pilot Indicator Control, C8862	DIG		P
	INCOS Power Supply, PP6664	PS	73H2500	PS
	Search Stores Decoder, KY747	DIG	73H3100	SSD
	Tacco and Senso Indicator Control, C8860 & C	DIG	73H1100 73H4200	TS
	Wing Command Sig Decoder, KY745 ( )	DIG	73H2200	WD
Mission Avionics	Analog Tape Recorder Reproducer Set, AN/ASH27			ATR/
	Magnetic Tape Transport, RD349	AN	7362100	TT
	Tape Transport Interface Unit, MX8959	AN	7382200	IU
	Sonobuoy Radio Receiver Set, AN/ARR76			SRX/
	Sonobuoy Receiver, R1741	RF	739C100	RCVR
	RF Amplifier, AM6418	RF	739C300	AMP
	Sonobuoy Bearing and Range Receiver, R1768/ARS2	RF	734P100	SRS
	Magnetic Anomaly Detection			MAD/
	Analog-to-Digital Converter, CV2881/AS	DIG	73X2600	CONV
	Acoustic Data Processor, OL82/AYS			ADP/
	Signal Data Converter, CV2882 ( )	DIG	73B3100	SDC
	Signal Generator Spectrum Analyzer, SG962 ( )	DIG	73B3300	SGSA
	Spectrum Analyzer Converter, CV2883	DIG	73B3500	SAC
	Magnetic Drum Data Storage, MU576	DIG	73B3A00	DRUM
	Drum Power Supply, PP6671	PS	73B3B00	PS
	Sono Monitor Panel, SB3593	AN	73B3C00	SMP
	Sonar Data Computer, CP1140	DIG	73B3D00	COMPO
	Forward Looking Infrared Radar, OR89 ( )/AA			FLIR/
	Video Converter and Power Supply, PP6611/AA	PS	7331400	PS
	Control Converter, C8759 ( )/AA	DIG	7731500	CONV
	Electronic Countermeasures Receiving Set, AN/ALR47			ESM/
	Receiver, R1742	RF	768G300	RCVR
	Signal Comparator, CM416	DIG	7383100	COMPA
Radar	Radar Interface Unit, C8788/AP	DIG	729F200	RIU
Airframe	Sppedbrake/Trum Control Unit	DIG	1422200	STCU
	Wing/Empennago Deice Timing Control	DIG	4131400	DEICE/TIM
	Windshield Temperature Controller	AN	4941100 4941200	WTC
	Automatic Flight Control Set, AN/ASW33			AFCS/
	Roto Gyroscope, CN1370	AN	5736400	GYRO
	Flight Data Computer, CP1074	AN	5736700	GDC
	Generator Control Unit	AN	4211400	GCU
DIM/FL	Dimmer/Flasher Control, Tail Light Sys.	AN	4413100	DIM/FL

*DIG = Digital, AN = Analog, RF = Radio Freq., PS = Power Supply.

TABLE 3. - S-3A EQUIPMENT CHARACTERISTICS, ATE SUPPORTED

DIGITAL EQUIPMENT

LRU	Weight lb	Volume in^3	Power Watts	LRU Pins	EMC	AEG	COMP	SRU Pins	Fail Modes	LNFAIL
Digital										
AACS	31	914	203	153	34	2060	3320	2166	18980	9.9
ADP/COMPU	48	2048	612	424	71	9332	6540	5594	99572	11.5
ADP/DRUM	47	1995	260	517	10	1195	1650	466	12750	9.5
ADP/SAC	43	2495	798	332	31	4335	3150	1992	45400	10.7
ADP/SDC	41	2048	684	442	46	3595	5000	2302	38358	10.6
ADP/SGSA	45	2494	810	412	30	4946	3800	2253	53700	10.9
AHRS/CONV	18	744	364	387	22	1322	1550	1260	10980	9.3
CC/ICS	6	183	44	53	9	188	260	159	1420	7.3
CC/IRC	14	440	114	111	17	401	820	745	7600	8.9
CC/SLU	44	2394	412	819	30	1923	5800	1923	27960	10.2
DEICE/TIM	3	138	168	80	5	358	360	58	1180	7.1
DMTU	20	914	65	51	17	711	1300	446	5800	8.7
DTS	32	538	125	280	31	1253	3000	1268	14240	9.6
ESM/COMPA	42	1710	550	227	20	885	2110	654	10700	9.3
FDIS/NDRC	28	748	102	487	43	2479	3020	2285	20050	9.9
FLIR/CONV	30	1498	200	117	22	548	1770	732	5590	8.6
INCOS/ACP	11	468	435	224	26	1308	990	887	8680	9.1
INCOS/BBD	7	404	14	170	13	324	845	378	3050	8.0
INCOS/C	13	622	86	95	16	490	394	263	3020	8.0
INCOS/P	4	170	49	42	5	338	312	54	2740	7.9
INCOS/SSD	8	585	590	165	14	414	740	445	3560	8.2
INCOS/TS	67	668	625	54	19	165	1170	420	2430	7.8
INCOS/WD	4	207	10	80	8	213	430	222	2010	7.6
INSI/CONT	7	379	49	199	14	357	360	370	2900	8.0
INSI/CONV	21	772	272	325	21	2321	2440	2085	20300	9.9
MAD/CONV	18	748	50	190	17	292	970	873	6510	8.8
RIU	43	1662	316	268	18	1367	3100	1604	23850	10.1
STCU	18	125	230	384	17	525	2260	603	6600	8.8
TDS/DGU	80	4888	750	292	43	5638	5610	6991	44130	10.7
DIG AV	27	1138	310	254	23.1	1699	2175	1362	17381	9.1

TABLE 3. - S-3A EQUIPMENT CHARACTERISTICS, ATE SUPPORTED (Continued)

NONDIGITAL EQUIPMENT

LRU	Weight lb	Volume in^3	Power Watts	LRU Pins	EMC	AEG	COMP	SRU Pins	Fail Modes	LNFAIL
Analog										
ADP/SMP	4	159	1	110	3	38	200	67	400	6.0
AFCS/FDC	58	2161	821	695	57	2437	17100	3255	32400	10.4
AFCS/GYRO	4	77	23	234	8	38	300	144	640	6.5
AHRS/GYRO	18	646	60	95	8	101	360	162	1100	7.0
ATR/IU	27	1330	642	316	20	1009	260	921	950	6.9
ATR/TT	87	4826	115	375	12	244	100	376	2700	7.9
DIM/FL	2	75	460	23	3	77	250	44	780	6.7
FDIS/HSI	8	285	39	86	8	71	400	186	900	6.8
FDIS/VDI	7	144	25	74	6	29	270	185	500	6.2
GCU	6	242	83	145	6	58	320	230	700	6.6
INCOS/BBDB	3	278	140	124	5	8	123	114	207	5.3
RAAWS/IND	11	44	19	38	3	60	320	63	700	6.6
TDS/ARU	48	3975	285	79	9	171	1200	400	2400	7.8
TDS/C	48	2080	525	86	13	206	1300	416	2750	7.9
TDS/P	34	1435	625	59	15	464	2500	718	5100	8.5
TDS/TS	67	5600	625	109	14	165	1280	420	2740	7.9
WTC	4	255	337	27	3	92	190	54	660	6.5
Analog AV	26	1389	284	157	11	310	1557	456	3272	7.1
Radio Freq										
Doppler	44	3904	165	80	16	505	510	685	5300	8.6
ESM/RCVR	25	627	330	64	11	151	720	210	1950	7.6
HF/AC	22	1127	136	51	7	190	600	126	1680	7.4
HF/PA	66	2367	605	124	20	437	1670	445	4260	8.4
HF/RT	28	914	193	117	18	684	3720	705	8130	9.0
RAAWS/RT	10	248	72	41	18	505	1800	330	5300	8.6
SRS	35	1539	150	175	33	734	2560	558	7540	8.9
SRX/RCVR	38	1829	240	141	47	983	4300	1460	12660	9.4
SRX/AMP	1	22	3	8	1	2	50	6	88	4.5
UHF/RT	32	998	968	94	21	366	2930	255	5610	8.6
RF AV	30	1358	286	89	19	456	1886	478	5252	8.1
Power Supply										
ADP/PS	51	1330	880	152	9	429	1160	280	4050	8.3
FLIR/PS	31	1174	300	103	16	187	870	220	2080	7.6
GPDC/PS1	33	920	1281	55	3	14	116	42	226	5.4
GPDC/PS2	33	920	1281	55	3	14	116	42	226	5.4
GPDC/PS-CP	7	118	710	37	3	18	150	60	320	5.8
GPDC/PS-IO	7	142	520	49	4	14	150	44	386	6.0
GPDC/PS-MEM	4	100	246	32	4	14	120	44	260	5.6
INCOS/PS	20	555	124	115	3	38	150	28	312	5.7
P.S. AV	23	657	668	75	6	91	354	95	983	6.2
Non-Dig AV	26	1213	372	119	12	301	1376	380	2482	7.2

TABLE 4. S-3A LRU TEST ATTRIBUTES, ATE SUPPORTED

DIGITAL EQUIPMENT

LRU	CKT Type	% BIT	Comp Dens No/Cu in	Tester Compatibility ID SRU	ID AEG	ID Comp	ID Val	ID CMPLX	Func Mod
Digital									
AACS	IC	0.4	3.6	21	262	139	286	3	1
ADP/COMPU	IC	3.3	3.2	38	1972	1276	2035	3	3
ADP/DRUM	IC	1.4	0.8	23	281	287	310	3	1
ADP/SAC	IC	5.3	1.3	20	223	248	248	3	3
ADP/SDC	IC	10.2	2.4	32	1108	682	1154	3	4
ADP/SGSA	IC	3.9	1.5	24	1024	665	1061	3	3
AHRS/CONV	IC	3.3	2.1	7	16	35	24	2	4
CC/ICS	HY	4.8	1.4	1	30	36	32	2	4
CC/IRC	IC	1.2	1.9	2	24	5	26	2	1
CC/SLU	IC	4.9	2.4	21	71	310	98	3	1
DEICE/TIM	HY	22.1	2.6	2	0	56	3	1	5
DMTU	HY	13.1	1.4	16	42	94	60	2	1
DTS	HY	5.8	5.6	6	34	68	41	2	1
ESM/COMPA	IC	3.3	1.2	7	16	44	24	2	3
FDIS/NDRC	IC	5.2	4.0	26	128	133	157	3	2
FLIR/CONV	HY	14.4	1.2	7	36	47	45	2	5
INCOS/ACP	IC	7.7	2.1	6	42	81	50	2	4
INCOS/BBD	HY	13.1	2.1	5	55	27	60	2	3
INCOS/C	IC	3.6	0.6	0	0	20	1	1	2
INCOS/P	IC	2.4	1.8	0	0	8	1	1	3
INCOS/SSD	IC	3.8	1.3	1	1	57	3	1	3
INCOS/TS	IC	7.8	1.8	0	0	30	1	1	4
INCOS/WD	HY	11.0	2.1	5	55	0	60	2	1
INSI/CONT	IC	11.2	0.9	14	18	20	32	2	5
INSI/CONV	IC	6.0	3.2	14	192	67	207	3	3
MAD/CONV	IC	11.5	1.3	15	69	60	85	2	1
RIU	IC	0.6	1.9	16	148	96	166	3	1
STCU	HY	12.0	18.1	6	12	88	20	2	4
TDS/DGU	IC	1.4	1.1	18	555	897	591	3	1
NONDIGITAL EQUIPMENT									
Analog									
ADP/SMP	HY	2.0	1.3	0	0	0	0	1	4
AFCS/FDC	IC	16.3	7.9	45	196	448	250	3	1
AFCS/GYRO	HY	9.6	3.9	3	3	42	7	1	1
AHRS/GYRO	HY	5.6	0.6	0	0	0	0	1	2
ATR/IU	IC	5.8	0.2	6	15	66	24	2	5
ATR/TT	HY	3.8	0.1	9	2	74	13	.1	5
DIM/FL	HY	0.1	3.3	2	0	56	3	1	3

ID COMPLX: Simple = 1, Numerical = 2, Complex = 3

Func Mod: 5 Good, 3 Avg, 1 Poor

TABLE 4. S-3A LRU TEST ATTRIBUTES, ATE SUPPORTED (Continued)

NONDIGITAL EQUIPMENT

LRU	CKT Type	% BIT	Comp Dens No/Cu in	Tester Compatibility ID SRU	ID AEG	ID Comp	ID Val	ID CMPLX	Func Mod
Analog (Cont)									
FDIS/HSI	DIS	1.7	1.4	0	0	0	0	1	5
FDIS/VDI	HY	25.6	1.9	0	0	0	0	1	5
GCU	DIS	7.7	1.3	0	0	6	0	1	4
INCOS/BBDB	DIS	0.1	0.4	0	0	18	0	1	5
RAAWS/IND	DIS	10.0	7.3	0	0	3	0	1	5
TDS/ARU	DIS	5.9	0.3	18	555	897	591	3	5
TDS/C	HY	3.9	0.6	18	555	897	591	1	5
TDS/P	DIS	4.3	1.7	18	555	897	591	3	5
TDS/TS	HY	14.1	0.2	18	555	897	591	3	5
WTC	HY	21.8	0.7	2	0	56	3	1	1
Radio Freq									
Doppler	HY	9.2	0.1	0	0	11	0	1	5
ESM/RCVR	HY	1.0	1.1	0	0	16	0	1	4
HY/AC	HY	8.2	0.5	12	0	11	12	2	4
HF/PA	DIS	8.8	0.7	12	0	11	12	2	4
HF/RT	HY	10.7	4.1	0	0	0	0	1	1
RAAWS/RT	HY	10.6	7.3	133	174	150	310	3	1
SRS	HY	4.4	1.7	17	7	18	24	2	5
SRX/RCVR	IC	4.6	2.4	3	36	29	39	2	4
SRX/AMP	DIS	0.1	2.3	3	36	29	39	2	5
UHF/RT	HY	9.5	2.9	1	1	17	2	1	4
Power Supply									
ADP/PS	HY	1.0	0.9	0	0	25	1	1	3
FLIR/PS	HY	5.1	0.7	2	18	46	21	2	4
GPDC/PS1	DIS	14.1	0.1	2	0	16	2	1	3
GPDC/PS2	DIS	14.1	0.1	2	0	16	2	1	3
GPDC/PS-CP	DIS	8.5	1.3	2	0	49	3	1	4
GPDC/PS-IO	DIS	6.4	1.1	2	0	49	3	1	3
GPDC/PS-MEM	DIS	8.4	1.2	2	0	49	3	1	3
INCCS/PS	HY	1.0	0.3	0	0	14	0	1	5

ID COMPLEX: Simple = 1 Func Mod: 5 Good
Numerical = 2 3 Avg
Complex = 3 1 Poor

TABLE 5. - S-3A OTHER TEST ATTRIBUTES, ATE SUPPORTED DIGITAL EQUIPMENT

Intermediate Level				Test Ambiguity					
				Design – %			Actual – %		
LRU	Tests	Fault Det Run-Min	Run Pred. Hrs	1 SRU	2 SRU	3 SRU	1 SRU	2 SRU	3 SRU
Digital									
AACS	1079	29	1.5	77	90	100	39	52	71
ADP/COMPU	20568	93	3.6	82	99	100	35	55	65
ADP/DRUM	1137	41	1.9	64	95	100	11	43	69
ADP/SAC	660	29	1.5	86	98	100	31	52	65
ADP/SDC	4780	85	3.3	91	95	100	35	53	66
ADP/SGSA	1017	38	1.8	84	98	100	32	56	71
AHRS/CONV	810	14	1.0	90	99	100	32	49	60
CC/ICS	708	8	0.8	91	98	100	37	63	73
CC/IRC	250	32	1.6	43	91	100	32	51	70
CC/SLU	992	62	2.6	75	90	98	30	53	65
DEICE/TIM	156	38	1.8	99	100	100	44	68	80
DMTU	430	30	1.5	55	85	100	67	78	90
DTS	400	15	1.0	63	93	100	41	49	82
ESM/COMPA	1118	35	1.7	80	97	100	43	70	86
FDIS/NDRC	1058	35	1.7	83	93	100	37	54	72
FLIR/CONV	550	8	0.8	97	100	100	33	59	71
INCOS/ACP	3093	57	2.4	91	98	100	36	58	70
INCOS/BBD	472	5	0.7	88	100	100	43	54	79
INCOS/C	352	12	0.9	80	91	100	39	56	74
INCOS/P	207	6	0.7	84	98	100	41	73	92
INCOS/SSD	729	33	1.6	85	95	100	41	62	75
INCOS/TS	4915	21	1.2	91	99	100	42	61	76
INCOS/WD	179	3	0.6	76	98	100	35	61	79
INSI/CONT	375	8	0.8	98	100	100	45	73	82
INSI/CONV	2783	28	1.4	84	98	100	31	53	70
MAD/CONV	706	15	1.0	71	100	100	34	53	70
RIU	1810	49	2.1	61	96	98	35	53	69
STCU	1023	26	1.4	91	99	100	34	60	72
TDS/DGU	1928	45	2.0	81	96	98	32	50	57
Averages	1872	31	1.5	81			37		

TABLE 5. - S-3A OTHER TEST ATTRIBUTES, ATE SUPPORTED (Continued)

NONDIGITAL EQUIPMENT

Intermediate Level				Test Ambiguity					
				Design – %			Actual – %		
LRU	Tests	Fault Det Run-Min	Run Pred. Hrs	1 SRU	2 SRU	3 SRU	1 SRU	2 SRU	3 SRU
Analog									
ADP/SMP	107	12	0.9	90	97	100	33	67	75
AFCS/FDC	4186	61	2.5	59	97	99	34	59	76
AFCS/GYRO	83	7	0.7	64	100	100	35	58	74
AHRS/GYRO	106	11	0.9	85	91	100	39	52	79
ATR/IU	892	27	1.4	98	100	100	41	68	79
ATR/TT	230	54	2.3	95	100	100	25	56	84
DIM/FL	32	4	0.6	84	100	100	58	75	92
FDIS/HSI	79	14	1.0	ETE	–	–	ETE	–	–
FDIS/VDI	100	7	0.7	ETE	–	–	ETE	–	–
GCU	284	19	1.1	91	100	100	39	63	85
INCOS/BBDB	83	2	0.6	99	100	100	83	100	100
RAAWS/IND	88	10	0.8	ETE	–	–	ETE	–	–
TDS/ARU	323	15	1.0	96	100	100	43	53	75
TDS/C	740	37	1.7	98	100	100	43	58	74
TDS/P	736	59	2.5	98	100	100	38	62	72
TDS/TS	1091	26	1.4	98	100	100	39	58	71
WTC	128	19	1.1	73	94	100	28	47	53
Average	546			88			41		
Radio Freq									
Doppler	893	14	1.0	99	100	100	54	74	84
ESM/RCVR	732	17	1.1	92	99	100	48	67	78
HF/AC	116	12	0.9	84	100	100	57	74	87
HF/PA	101	8	0.8	93	100	100	30	45	49
HF/RT	231	13	0.9	70	98	100	41	59	70
RAAWS/RT	513	19	1.1	62	92	100	35	55	68
SRS	892	47	2.1	98	100	100	32	61	81
SRX/RCVR	284	92	3.6	90	98	100	40	76	85
SRX/AMP	10	2	0.6	ETE	–	–	ETE	–	–
UHF/RT	496	9	0.8	90	99	100	40	63	79
Average	427			86			42		
Power Supply									
ADP/PS	162	13	0.9	86	97	100	100	100	100
FLIR/PS	114	18	1.1	90	100	100	23	54	70
GPDC/PS1	86	6	0.7	91	91	100	63	88	100
GPDC/PS2	86	6	0.7	91	91	100	60	100	100
GPDC/PS-CP	100	3	0.6	92	100	100	71	93	100
CPDC/PS-IO	132	3	0.6	85	100	100	100	100	100
GPDC/PS-MEM	93	3	0.6	90	100	100	99	100	100
INCOS/PW	153	5	0.7	99	100	100	27	33	67
Average	116			91			55		
NONDIG Avg	414			88			45		

TABLE 6. - S-3A FIELD EXPERIENCE, ATE SUPPORTED

59,619 FLIGHT HOURS, 1977

DIGITAL EQUIPMENT

LRU	TPS Devel Hours	TPS Station Hours	Maint Manhours			AV Elapsed Maint Time-Hrs		
			O-Level	I-Level	Total	O-Level	I-Level	Total
Digital								
AACS	12349	1368	1.9	12.4	14.3	1.1	3.2	4.3
ADP/COMPU	15841	5957	2.5	13.5	16.0	1.4	5.4	6.8
ADP/DRUM	8690	1257	2.8	15.6	18.4	1.6	3.9	5.5
ADP/SAC	8744	1072	2.5	14.4	16.9	1.4	3.8	5.2
ADP/SDC	13481	2883	2.7	11.4	14.1	1.5	3.3	4.8
ADP/SGSA	9747	1233	2.5	12.5	15.0	1.4	4.3	5.7
AHRS/CONV	10591	1413	2.0	7.7	9.7	1.2	3.1	4.3
CC/ICS	3521	372	1.5	8.0	9.5	1.0	2.6	3.6
CC/IRC	4248	497	1.5	11.5	13.0	1.0	3.3	4.3
CC/SLU	23282	2893	1.9	12.9	14.8	1.2	3.8	5.0
DEICE/TIM	1811	157	5.6	8.1	13.7	2.5	1.8	4.3
DMTU	8910	1435	1.8	8.5	10.3	1.1	2.5	3.6
DTS	12372	2107	2.6	12.1	14.7	1.4	3.2	4.6
ESM/COMPA	9016	2454	2.5	9.6	12.1	1.5	2.9	4.4
FDIS/NDRC	10810	1199	1.9	12.5	14.4	1.2	3.3	4.5
FLIR/CONV	9792	1491	2.1	9.4	11.5	1.2	3.2	4.4
INCOS/ACP	11894	1749	1.7	11.3	13.0	1.0	2.8	3.8
INCOS/BBD	5488	681	2.0	11.1	13.1	1.1	2.0	3.1
INCOS/C	4089	542	1.8	12.1	13.9	1.1	3.2	4.3
INCOS/P	3505	488	1.8	7.2	9.0	1.2	3.1	4.3
INCOS/SSD	7773	1167	1.7	10.3	12.0	1.1	2.6	3.7
INCOS/TS	5365	681	2.7	12.0	14.7	1.5	3.8	5.3
INCOS/WD	4026	423	2.1	10.3	12.4	1.2	2.3	3.5
INSI/CONT	4866	282	2.0	12.0	14.0	1.3	3.7	5.0
INSI/CONV	11881	1291	2.1	14.5	16.6	1.3	3.4	4.7
MAD/CONV	8958	1224	2.0	9.0	11.0	1.2	2.6	3.8
RIU	17202	3103	2.4	15.7	18.1	1.4	3.7	5.1
STCU	4608	159	2.1	14.6	16.7	1.2	3.9	5.1
TDS/DGU	18690	2759	3.1	11.5	14.6	1.6	1.9	3.5
Dig Average	9362	1460	2.3	11.4	13.7	1.3	3.2	4.5
ATE Tester: AN/USM-247 VAST								

TABLE 6. - S-3A FIELD EXPERIENCE, ATE SUPPORTED (Continued)

59,619 FLIGHT HOURS - 1977

NONDIGITAL EQUIPMENT

LRU	TPS Devel (MH)	TPS Dev Station (Hrs)	Maint Manhours O-Level	Maint Manhours I-Level	Maint Manhours Total	Elapsed Maint Time-Hr O-Level	Elapsed Maint Time-Hr I-Level	Elapsed Maint Time-Hr Total
Analog								
ADP/SMP	2142	349	1.9	7.0	8.9	1.1	2.9	4.0
AFCS/FDC	20,046	2043	2.4	12.8	15.2	1.4	5.9	7.3
AFCS/GYRO	1363	132	2.7	8.9	11.6	1.6	2.4	4.0
AHRS/GYRO	3323	375	3.3	4.0	7.3	1.9	3.8	5.7
ATR/IU	5287	615	2.1	11.3	13.4	1.2	4.7	5.9
ATR/TT	6018	681	2.5	11.2	13.7	1.3	3.7	5.0
DIM/FL	1757	188	2.6	2.9	5.5	1.7	1.9	3.6
FDIS/HSI	3422	242	2.5	2.5	5.0	1.5	4.1	5.6
FDIS/VDI	2387	190	2.3	2.2	4.5	1.4	3.0	4.4
GCU	4393	647	2.3	1.0	3.3	1.5	3.0	4.5
INCOS/BBDB	356	35	1.8	4.3	6.1	1.0	1.6	2.6
RAAWS/IND	2726	257	1.5	2.0	3.5	1.0	2.8	3.8
IDS/ARU	4602	642	2.3	7.3	9.6	1.3	3.4	4.7
IDS/C	5335	666	2.2	9.1	11.3	1.3	4.3	5.6
TDS/P	5522	779	2.2	7.6	9.8	1.2	3.5	4.7
TDS/TS	5208	667	2.4	8.5	10.9	1.3	4.3	5.6
WTC	2577	423	1.7	7.8	9.5	1.1	3.2	4.3
AV	4498	525	2.3	6.5	8.8	1.4	3.4	4.8
Radio Req								
DOPPLER	6685	846	2.9	13.0	15.9	1.5	3.3	4.8
ESM/RCUR	7312	845	6.1	11.2	17.3	2.1	3.7	5.8
HF/AC	3050	307	3.1	10.4	13.5	1.6	4.2	5.8
HF/PA	3374	342	2.3	15.8	18.1	1.3	3.3	4.6
HF/RT	6186	789	2.2	15.0	17.2	1.3	2.1	3.4
RAAWS/RT	6937	852	1.5	9.9	11.4	1.0	3.7	4.7
SRS	9527	1470	2.4	1.2	3.6	1.3	3.4	4.7
SRX/RCUR	9342	1519	1.8	11.6	13.4	1.1	1.4	2.5
SRX/AMP	889	80	1.9	2.2	4.1	1.3	3.8	5.1
UHF/RT	7604	953	1.5	16.2	17.7	0.9	0.2	1.1
AV	6086	800	2.9	11.7	14.6	1.3	2.8	4.1
Power Supply								
ADP/PS	2966	329	2.9	10.4	13.3	1.7	2.6	4.3
FLIR/PS	3187	343	2.1	13.6	15.7	1.2	3.5	4.7
GPDC/PSI	1947	249	3.6	8.7	12.3	2.2	2.7	4.9
GPDC/PS2	1792	249	3.3	9.7	13.0	1.9	3.1	5.0
GPDC/PS-CP	1660	188	4.2	5.0	9.2	2.5	3.2	5.7
GPDC/PS-10	1971	260	5.1	3.6	8.7	2.4	2.5	4.9
GPDC/PS-MEM	1301	104	3.3	5.1	8.4	2.1	4.3	6.4
INCOS/PS	1778	220	2.3	8.1	10.4	1.2	4.0	5.2
AV	2076	242	3.4	8.0	11.4	1.9	3.2	5.1
NON-DIG AV	4398	539	2.6	8.0	10.6	1.5	3.2	4.7

ATE Tester. AN/USM-247 VAST

TABLE 7. - S-3A EQUIPMENT - MTE SUPPORTED

Function	Nomenclature	Type	WUC	Acronym
Data Processing	Tachometer Ind. - ERU 17/A	AN	5131100	TACI
	Fan Speed Ind. - ERU 9/A	AN	5132100	FANI
	ITT Ind. - EHU 37A/A	AN	5133100	ITTI
	Fuel Flow Ind - EFU 41/A	AN	5134100	FFI
	Ind Panel Assy.	AN	5141100	INDA
Navigation	Tacan Rcvr - Trans-RT1022/ARN84	RF	713C100	TACX
	D/F Receiver - R139/ARN83	RF	7148100	DFR
Communications	Freq Select Control - C8881/ARC156	AN	6327400	FSC
	Radio Rcvr - RT1379( )/ARA63	RF	71D1100	RCVR
	Pulse Decoder - KY651( )/ARA63	DIG	71D1200	DCDR
Radar	Radar Power Supply - PP6633/APS-116	PS	727H100	RAPS
	Radar Exciter Synchronizer-SN460/APS-116	RF	727H200	RAES
	Radar Transmitter - T1203/APS-116	RF	727H300	RATX
	Radar RCVR - R1747/APS-116	RF	727H400	RARC
	Radar Beacon R/T - RT1028/APN202	RF	729D100	RBRT
	Sig Data Conv Storer - CV2852( )/AP	AN	729F100	RSDC
Mission Avionics	FLIR Viewer - IP1069( )/AA	AN	7731100	FLVW

TABLE 8. - S-3A EQUIPMENT CHARACTERISTICS AND EXPERIENCE - MTE SUPPORTED
59,619 FLIGHT HOURS, 1977

LRU	Weight lbs	Vol in^3	SRU	EMC	Maintenance Manhours		Elapsed Maint. Time-hrs	
					O-Level	I-Level	O-Level	I-Level
TACI	2.5	59	3	2	1.5	0.4	1.0	0
FANI	2.4	59	3	2	3.0	0.1	1.6	0
ITTI	2.4	59	3	2	2.0	0.4	1.2	0
FFI	2.4	59	3	2	1.5	0.5	1.0	0
INDA	2.6	59	5	3	4.4	0.5	1.8	0
TACX	33.2	1065	10	23	1.8	3.6	1.1	9.1
DFR	9.2	240	11	10	1.6	14.8	1.0	10.3
FSC	3.3	77	2	2	1.3	4.8	0.9	0.3
RCVR	4.5	112	3	2	5.1	4.9	3.0	3.8
DCDR	6.9	31	3	4	3.1	6.4	1.8	10.1
RAPS	42.3	1857	18	17	2.7	13.6	1.5	5.9
RAES	84.4	1775	30	29	3.9	16.2	2.0	10.5
RATX	1168.	5614	6	11	4.8	31.1	2.3	26.3
RARC	5.4	1949	24	21	4.1	29.2	2.1	11.7
RBRT	5.5	131	5	4	2.5	14.9	1.4	4.1
RSDC	42.9	2410	19	19	2.4	22.4	1.4	23.2
FLVW	169.	9999	25	50	8.0	22.4	3.6	77.8
AVG	93	1521		12	3.2	11.0	1.7	16.1

2.3.3 C-5A Data

Table 9 identifies the 23 LRUs surveyed from the C-5A avionics. The sample includes navigation, computers, communication, radar, and the MADAR test system. The malfunction Detection, Analysis, and Recording System (MADARS) is used as on-board test equipment to record and identify failures in flight. The 10 types of LRUs in the MADARS are supported at the I-Level using ATE, the AN/UG 2395BA01 tester. Twelve ATE supported and eleven MTE supported LRUs were included in the sample. Table 10 shows the equipment characteristics and experience for the period of March to December 1977. The 36,290 flight hours maintenance records are from the USAF 66-1 reporting system.

2.3.4 P-3C Data

Table 11 identifies the 13 LRUs from the P-3C avionics. The P-3C avionics is isolated to the SRU on board the aircraft and repaired at the depot, thus there is no I-Level data. Data were collected using the same maintenance reporting system (3M) used for the S-3A. Table 12 shows the equipment characteristics and experience for the period from October 1977 to September 1978, including 104,823 flight hours.

2.3.5 MK-86 Data

Table 13 identifies the shipboard radar from the MK-86 fire control system. This sample is twelve racks of shipboard equipment with 50,622 operating hours for the period from October 1977 to September 1978. Maintenance reporting was from the US Navy shipboard Maintenance Data System (MDS). The MK-86 includes BIT to detect failures at the O-Level. Local built-in test features are used to isolate the failure within the rack to a group of SRUs. Maintenance time is recorded as average elapsed time, or EMTO for comparison with the avionics systems.

TABLE 9. - C-5A EQUIPMENT

Function/LRU	Type	WUC	Acronym
Navigation and Computers			
CNTL Air Data Cmptr	DIG	51BA0	CADC
Autoload DISTR CMFTR	DIG	52PA0	ALDCS
Madar System		55A00	
SIG ACQ Remote-Auto	AN	55A00	SAR-A
SIG ACQ Remote-Man	AN	55AC0	SAR-M
MAMR Data Recorder	AN	55AE0	MDR
CNTL & SEQ Unit	DIG	55AG0	CSU
Oscilla/Dig Readout Unit	AN	55AJ0	ODRU
CNTRL MUX Adapter	DIG	55AL0	CMA
Printout Unit	AN	55AR0	POU
Manual Multiplex	DIG	55AT0	MMUX
Dig Computer	DIG	55AV0	DCOMP
Data Retrieval Unit	DIG	55AY0	DRU
Communications			
HF RCVR/Transmitter	RF	61AA0	HF/RT
HF ANT Coupler	RF	61AC0	HF/COUP
UHF RCVR/XMTR	RF	63AA0	UHF/RT
Inertial Doppler NAV-IDNE			
Indicator Panel	AN	72AA0	IDNE/IND
Power Supply	PS	72AC0	IDNE/TS
PRI & AUX CMPTR	DIG	72AE0	DNE/CMPTR
Doppler Radar	RF	728BK0	IDNE/RAD
Inert MEAS Unit	AN	728BP0	IDNE/IMU
PRI & AUX A/D Conv.	DIG	72BZ0	IDNE/CONV
Multimode Radar-MMR			
Ku Band Ant/RCVR	RF	72DA0	MMR/KU RCVR
Distribution Unit	AN	72DG0	MMR/DISTR

TABLE 10. - C-5A EQUIPMENT CHARACTERISTICS AND EXPERIENCE

MARCH TO DECEMBER 1977, 36,290 FLIGHT HOURS

LRU	Weight lb	Power Watts	SRU	I-Level Support	Maintenance Manhours		Elapsed Maintenance Time-Hr	
					O-Level	I-Level	O-Level	I-Level
CADC	35	120	11	ATE	2.6	10.9	1.3	8.3
ALDCS	23	300	14	ATE	2.8	5.8	1.3	3.2
SAR-A	3.8	4	7	ATE	4.9	4.8	2.4	2.6
SAR-M	4.0	7	8	ATE	1.5	0.8	0.8	0.8
MDR	31	150	14	ATE	2.3	5.6	1.2	3.8
CSU	40	330	33	ATE	2.4	6.7	1.3	4.6
ODRU	42	200	17	ATE	2.4	7.4	1.3	4.6
CMA	40	410	21	ATE	2.3	4.8	1.3	2.8
POU	17	150	5	ATE	1.9	4.0	1.1	2.6
MMUX	15	410	11	ATE	2.2	3.9	1.2	2.2
D COMP	38	6	5	ATE	2.2	13.0	1.2	11.7
DRU	43	150	10	ATE	2.4	5.9	1.3	3.5
ATE AVG	27.7	186.4	13		2.5	9.1	1.3	4.2
HF/RT	13	2500	10	MTE	2.5	7.0	1.3	4.2
HF/COUP	74	46	9	MTE	2.8	7.8	1.4	4.4
UHF/RT	29	370	11	MTE	2.2	8.7	1.2	4.8
IDNE/IND	2	96	5	MTE	2.3	6.6	1.2	5.3
IDNE/PS	51	500	13	MTE	2.4	15.1	1.2	14.0
IDNE/CMPTR	58	345	6	MTE	2.6	8.3	1.4	6.8
IDNE/RAD	21	270	4	MTE	2.5	7.6	1.3	6.2
IDNE/IMU	75	413	11	MTE	4.1	7.9	2.1	5.5
IDNE/CONV	15	130	9	MTE	2.3	9.8	1.3	8.5
MMR/KU RCVR	93	1000	10	MTE	8.0	25.9	4.0	16.8
MMR/DISTR	37	450	8	MTE	3.9	11.3	2.0	6.7
MTE AVG	42.5	556.4	8.7		3.2	10.5	1.7	7.6
TOTAL AVG	34.8	363.3	11.0		2.8	9.8	1.5	5.8

TABLE 11. - P-3C EQUIPMENT

Function	Nomenclature	Type	WUC	Acronym
Navigation	Radar Computer Tracker CP-919/APN-187	RF	723A1	RCTR
	Inertial Nav Computer CP-924/ASN 84	DIG	734F7	INCP
Communications	HF Receiver-Transmitter RT1100/ARC-161	RF	612M1	HFRT
	UHF Receiver-Transmitter RT932B/ARC-143	RF	632K1	UFRT
	Secure-Unsecure Amplifier AM4964/AIC-22(V)	ANAL	6422E	SUAM
Data Processing	Data Analysis Logic Unit #1 MX8023A/AYA-8	DIG	73661	DALI
	Digital Data Computer CP-901/ASQ-114(V)	DIG	73671	DDCP
	Multipurpose Data Display IP 917/ASA-70	ANAL	732B1	MPDD
	Radar Scan Converter CV 2425/ASA-69	ANAL	72812	RSCV
Mission Avionics	Signal Data Recorder RO-480/AQA-7(V)	ANAL	7378X	SDRR
	Digital Interface Unit J3346/AQA-7(V)	DIG	73791	DIU
	Spectrum Analyzer-Quantizer TS 3542/AQA-7(V)	ANAL	7378T	SAQ
	Cass Radio Transmitter	RF	69293	CADT

TABLE 12.- P-3C EQUIPMENT CHARACTERISTICS AND EXPERIENCE

OCT 77 TO SEPT 78, 104,823 FLIGHT HOURS

LRU	Weight lbs	Vol in^3	Power Watts	SRU	EMC	O-Level Maint Manhours	O-Level Elapsed Maint Time-Hr
RCTR	17	612	182	9	7	2.5	1.6
INCP	21	646	290	20	19	6.1	2.1
HFRT	32	1543	3000	10	9	2.1	1.4
VFRT	36	1217	800	4	15	2.0	1.3
SUAM	2	37	50	3	2	2.2	1.5
DAL1	135	9171	353	27	24	6.8	3.0
DDCP	345	20763	1071	10	7	5.6	3.5
MPDD	260	38367	500	5	31	3.2	2.1
RSCV	75	4867	200	18	16	1.8	1.4
SDRR	102	8410	200	7	5	3.3	1.8
DIU	16	1043	40	6	5	3.6	2.4
SAQ	33	2603	200	7	6	2.3	1.8
CAST	9	480	400	5	7	3.5	2.5
AVG	83	6905	560		12	3.5	2.0

TABLE 13. MK 86 EQUIPMENT AND EXPERIENCE

OCT 77 TO SEPT 78, 50622 HOURS

Unit	Name	Equip Type	Weight lbs	Vol in^3	Power Watts	EMC	% BIT	AVG Maint Time-Hr
6	Sig Data Converter	AN	450	57684	1250	178	4	1.9
10	Radar Receiver	RF	412	55890	525	28	32	3.8
11	Electronic Freq CNTL	RF	399	60800	965	32	34	2.5
12	Radar Transmitter	RF	458	206720	1658	29	33	6.3
13	Radar Antenna	RF	920	227200	805	13	0	6.5
17	Radar Antenna	RF	4015	1142400	254	17	0	1.6
18	Radar Receiver	RF	792	61320	527	93	8	2.1
19	Radar Transmitter	RF	643	49056	4256	12	17	3.3
21	Antenna Control	AN	437	54188	12750	13	22	3.0
22	Sig Data Converter	DIG	366	54188	230	146	20	14.7
23	Power Dist. CNTL	PS	215	29946	345	4	0	1.0
25	Video Processor	DIG	418	57684	460	207	11	2.1
AVG			794	171000	2002	64	15	4.1

3. FIELD SURVEY RESULTS

The results of the field survey of three airborne and one shipboard system are presented in this section. The systems described in the previous sections were analyzed to identify the major elements which impact testability and the resultant life cycle cost (LCC) for cost prediction of new designs. The intermediate level (I-level) test program development costs are examined in detail for the S-3A Viking system. Maintenance experience for all four systems is analyzed to determine predictors for preliminary and final design phases of acquisition.

3.1 Development Costs

The test program set (TPS) development costs for the S-3A system are presented in section 2. They include the TPS development cost (TPSHRS) in manhours and the test development station hours (STAHRS) for 64 LRUs. This section analyzes the impact of Unit-Under-Test (UUT) design characteristics on the development costs and derives the contributing effects of test attributes to TPSHRS and STAHRS.

3.1.1 Test Program Set Development

The impact of equipment type on the UUT design parameters showed that the TPSHRS could be more accurately evaluated by segregating digital from nondigital equipment. Digital LRUs are those units with over 51 percent digital SRUs, excluding power supplies and chassis. The remaining equipment types, analog, radio frequency, and power supplies were found to correlate as a single group. RF units with frequencies over 10 Gigahertz show some of the traits of complex digital LRUs. The digital group contains discrete and MSI integrated circuits. No LSI integrated circuits are used in the S-3A data base.

The digital group includes 29 LRUs with full fault isolation testing to identify malfunctions to the SRU level. The nondigital group includes 17 analog, 10 RF and 8 power supplies. Of the 35 nondigital LRUs, four are fault detection (end-to-end) testing only and the remaining 31 contain full diagnostics.

3.1.1.1 Derivation of TPSHRS. - The optimum combination of UUT characteristics were derived from the S-3A data base to develop a method for prediction of future system performance. The SPSS [2] software technique was used for the analysis. Successive comparisons were made for all UUT characteristics described in paragraph 2.2.1. The highest coefficient of determination (R^2) was selected for a group of prime equipment parameters whose multiple regression continued to reduce the standard error. In both digital and non-digital cases, four characteristics were required to define the most accurate linear correlation of elements with experienced TPSHRS. The following multiple linear regression equations were derived:

(Digital, R^2 = 0.828, std error = 2271)

$$\text{TPSHRS} = -11831 + 2.146\,(\text{COMP}) - 1.963\,(\text{AEG}) + 1976\,(\text{LNFAIL}) + 1.337\,(\text{SRUPIN}) \tag{12}$$

(Nondigital, R^2 = 0.903, std error = 1202)

$$\text{TPSHRS} = -3193 + 82.3\,(\text{EMC}) + 0.469\,(\text{COMP}) + 774.1\,(\text{LNFAIL}) + 3.008\,(\text{LRUPIN}) \tag{13}$$

The above equations were used to determine the influence of each parameter to the total cost by computing the value of TPSHRS as each parameter was varied in range from minimum to maximum. The resultant influence is shown below:

	Digital	Nondigital
Components	27.5%	42.8%
Active Element Groups	36.7	-
Failure Modes	16.9	21.2
Active LRU pins	-	11.1
Total active SRU pins	18.9	-
Equivalent Module Count	-	24.8

Examination of these data shows that components and active stages of circuitry (active element groups) have the greatest influence on development costs for digital equipment. In the case of nondigital LRUs, components and equivalent module count (EMC) are more important than AEG, primarily due to packaging techniques. Digital circuitry is packaged by physical limiations of the ICs and their functional relationship. Nondigital circuits are usually packaged in a more signal oriented method, such as amplifiers, sources, etc. Failures are more easily identified at the SRU pin for digital circuits, thus digital circuits must rely on other techniques or extra test points to bring the critical monitoring points to the LRU interface.

The TPS costs were accumulated for each LRU in three phases:

- Test Requirement Analysis (TRA) - Acquire basic data on the UUT for test analysis, prepare test requirement documentation (TRD) including diagnostic flow charts (DFC) and test setup diagrams compatible with the tester. Digital TRA labor did not include the generation of stimulus/response patterns which were purchased from the supplier.
- Test Software Development (TPS Design) - Coding of test program and test instructions, debug and demonstration of TPS integrity to MIL-STD-2084 (AS) requirements.
- Interface Hardware Design - Documentation of interface device (ID) and fabrication of development model.

The following procedure was derived to normalize equations (12) and (13) for predicting TPS costs other than those of the S-3A data base. TPS costs were found to represent the following percentages of TPSHRS:

	Digital	Nondigital
TRA	28.6%	28.4%
Software design	31.7	38.4
Hardware design	39.7	33.2

These ratios were considered in the analysis of data using averaging techniques. The multiple regression of the basic TPSHRS with test attributes resulted in the identification of the range of development cost variation as each attribute was varied from minimum to maximum. In those cases in which the coefficient of determination (R^2) did not exceed the minimum requirement of 0.64 or the standard error did not successively decrease, averages were used to determine the range. The averages were normalized as a ratio of EMC or components to the TPSHRS. The following coefficients were derived from (1) multiple regression analysis, or (2) averaging data:

		Digital	Nondigital
K_{TC} -	Tester Compatibility IDVAL = IDAEG + IDCOMP/50 + LRUPIN/100		
	ID1, simple, IDVAL less than 10	0.000	0.000
	ID2, nominal, IDVAL 10.1 to 100	0.007	0.126
	ID3, complex, IDVAL, greater than 100	0.125(2)	0.157(1)
K_{MOD} -	Functional Modularity degree of packaging from		
	Good = 5	0.000	0.000
	Above average = 4	0.017	0.002
	Average = 3	0.033	0.005
	Below average = 2	0.050	0.071
	Poor = 1	0.066(1)	0.142(2)
K_{CKT} -	Circuit Type		
	at least 75% discrete	0.000	0.156
	hybrid of discrete and IC	0.000	0.094
	at least 75% IC,MSI	0.034(2)	0.000(2)
K_{DENS} -	Component Density		
	Low, less than 1 comp/cu. in.	0.000	0.000
	Medium, 1 to 3 comp/cu. in.	0.014	0.041
	High, greater than 3 comp/cu. in.	0.028(1)	0.083(2)
K_{ISOL} -	Fault Isolation		
	Fault detection only	0.000	0.000
	Fault isolation, Design		
	Ambiguity less than 60%	0.124	0.044
	61 to 80%	0.148	0.061
	81 to 90%	0.172	0.078
	91 to 95%	0.196	0.096
	greater than 95%	0.221(1)	0.119(1)

Source of data:

(1) Multiple regression analysis; (2) Averaging of data base

The UUT design coefficient, K_D, is:

$$K_D = \frac{1}{1 - (K_{TC} + K_{MOD} + K_{CKT} + K_{DENS} + K_{ISOL})} \qquad (14)$$

where coefficients are the same as those described above.

3.1.1.2 Final predictions. - The above coefficients were used to calculate the 64 LRU TPSHRS and were compared as a function of components to the actuals shown in figure 12. The general conclusion is that the formulas are acceptable for predicting future development costs for ATE supported LRUs.

Equations (12) and (13) were scaled to include K_D as a multiplier, yielding the following formula:

Digital, (R^2 = 0.828, std error = 2271)

$$\text{TPSHRS} = K_D[- 8163 +1.481 \text{ (COMP)} - 1.354 \text{ (AEG)} + 1563 \text{ (LNFAIL)} + 0.923 \text{ (SRUPIN)}] \qquad (15)$$

Nondigital, (R^2 = 0.903, std error = 1202)

$$\text{TPSHRS} = K_D[- 2143 + 0.315 \text{ (COMP)} + 55.2 \text{ (EMC)} + 519 \text{ (LNFAIL)} + 2.018 \text{ (LRUPIN)}] \qquad (16)$$

3.1.1.3 Preliminary predictions. - In the early phase of development, approximate data is available or estimated from similar UUTs to predict the order of magnitude of the TPS development costs. The design coefficient used for these predictions is the average complexity of digital K_D = 1.29 and nondigital at K_D = 1.52.

Digital, (R^2 = 0.696, std error = 3022)

$$\text{TPSHRS} = 2105 + 1.67 \text{ (VOLUME, cu. in.)} + 8.4 \text{ (LRUPIN)} + 84.6 \text{ (EMC)} - 2.61 \text{ (POWER, Watts)} \qquad (17)$$

Nondigital, (R^2 = 0.840, std error = 1494)

$$\text{TPSHRS} = 609 + 150 \text{ (EMC)} + 3.69 \text{ (LRUPIN)} \qquad (18)$$

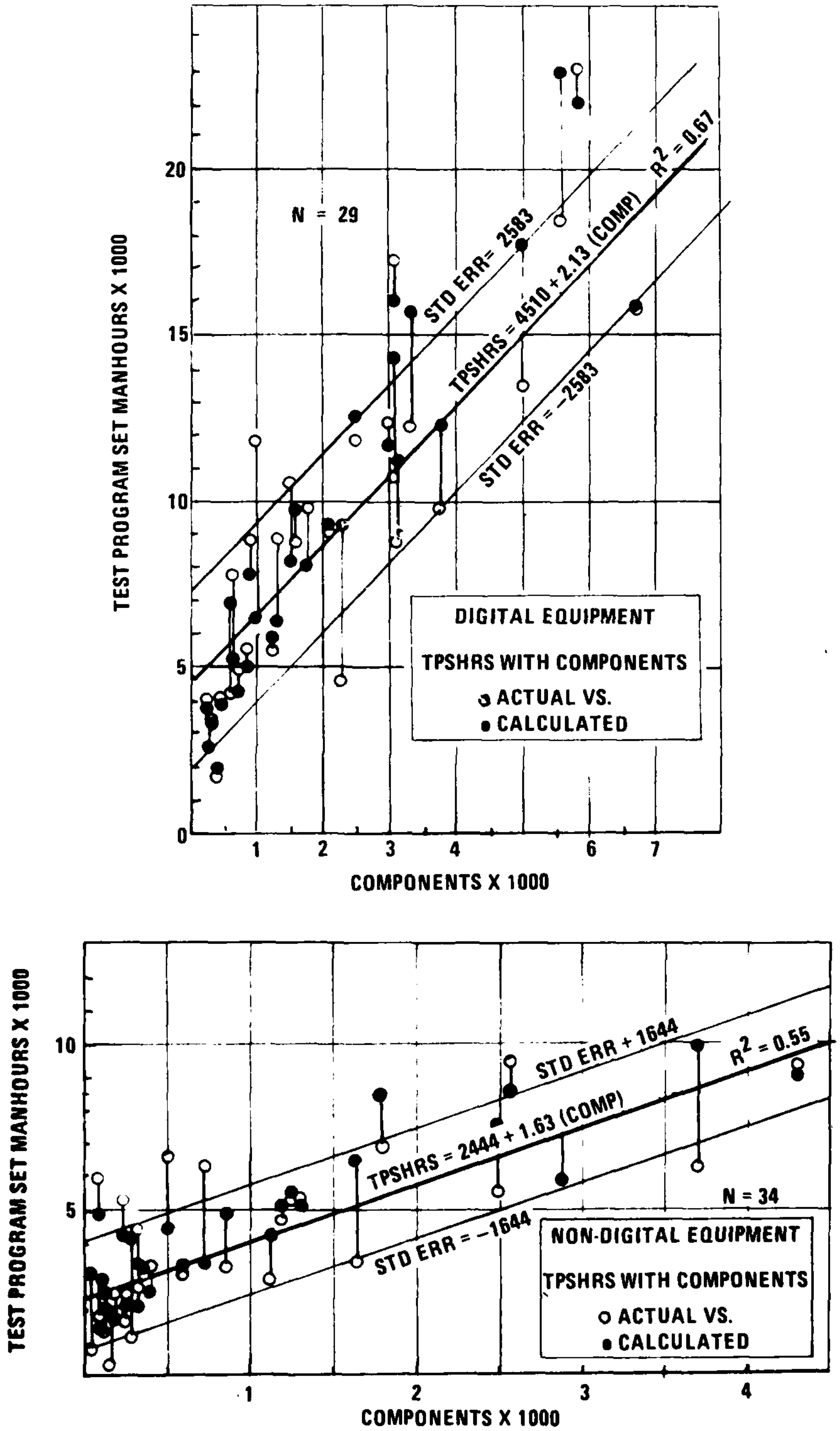


Figure 12. - Comparison of calculated and actual TPSHRS with components

3.1.2 Test Program Set Development Test Station Hours

A high correlation of STAHRS to TPSHRS was obtained for a single regression of all 64 LRUs. The number of actual test station hours needed to debug and demonstrate TPS quality was derived:

All Electronics (R^2 = 0.839, std error = 1646.7)

$$\text{STAHRS} = \frac{\text{TPSHRS} - 1805}{5.22} \tag{19}$$

The equation may be used for preliminary or final design predictions.

STAHRS were also derived from the UUT design characteristics:

Digital, (R^2 = 0.672, std error = 725)

$$\text{STAHRS} = 325.3 + 0.408\ (\text{COMP}) + 0.145\ (\text{AEG}) \tag{20}$$

Nondigital, (R^2 = 0.694, std error = 239)

$$\text{STAHRS} = -\ 612.2 + 0.0456\ (\text{COMP}) + 137.1\ (\text{LNFAIL}) + 0.550\ (\text{LRUPIN}) \tag{21}$$

3.2 Maintenance Experience

The analysis of maintenance manhours (MMH) and elapsed maintenance time (EMT) resulted in low correlation. Separate O-Level and I-Level correlations shown in tables 6, 8, 10, 12 and 13 were compared and are shown in figure 13. The results show that maintenance of both digital and nondigital equipment at both levels are the same.

3.2.1 Maintenance Manhours

3.2.1.1 Organizational level. - Low correlation was obtained from multiple regression analysis, therefore the maintenance manhours averages at O-Level (MMHO) are compared in figure 13. The average for all equipment is 2.5 hours. Table 6 shows the individual averages for the 64 S-3A LRUs supported by BIT. Table 10 shows a C-5A average of 2.5 hours for the BIT supported LRUs using the MADARS onboard test system. The average O-Level maintenance time for both systems is 2.8 hours. These systems represent two different generations of electronics. The S-3A uses more digital circuitry and MSI integrated circuits.

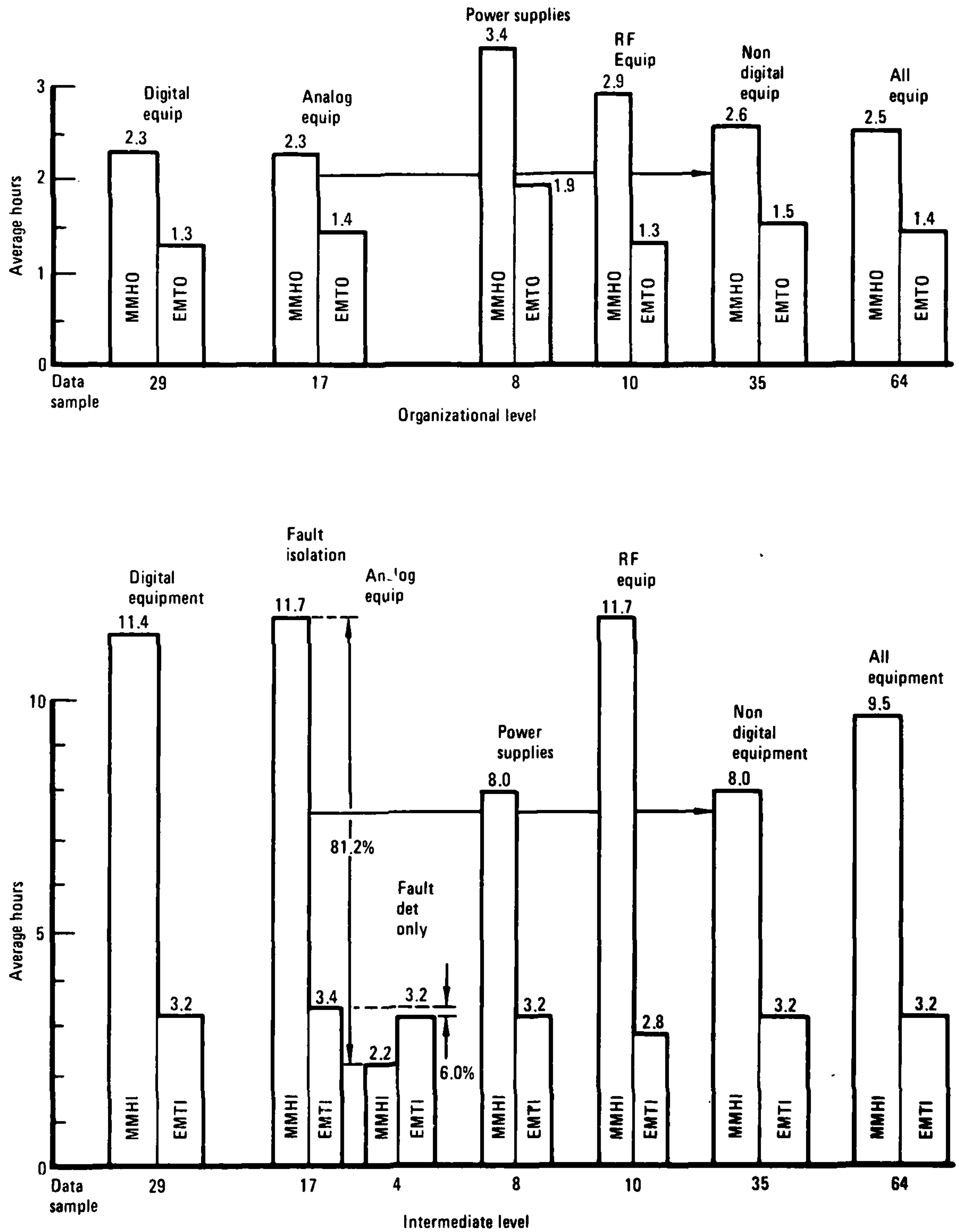


Figure 13. - S-3A Maintenance time averages.

The C-5A system represents a 10 year older design and utilizes more discrete circuitry packaged in cordwood or pre-integrated circuit packaging. The P-3C system average shown in table 12 is 3.5 hours and consists of a combination of older electronics and newer S-3A vintage. The next generation will use more compact integrated circuits, thus it can be assumed that a higher reliance on BIT will be mandatory to maintain or reduce the MMHO average test time.

3.2.1.2 Intermediate level. - The maintenance manhours at the I-Level are also shown in the figures and tables referenced in paragraph 3.2.1.1. The average MMHI is 9.3 hours for both systems, considering only ATE supported LRUs. The following relationships were derived from the SPSS analysis:

S-3A Digital, ATE supported, (R^2=0.597, std error=1.956)

$$\text{MMHI} = 3.848 + 0.730\ (\text{LNFAIL}) + 0.0037\ (\text{LRUPIN}) \qquad (22)$$

S-3A Nondigital, ATE supported, (R^2=0.446, std error=3.393)

$$\text{MMHI} = -5.421 + 1.888\ (\text{LNFAIL}) \qquad (23)$$

C-5A, ATE and MTE supported, (R^2=0.751, std error=2.741)

$$\text{MMHI} = 8.274 + 0.214\ (\text{Weight, lb}) - 0.0032\ (\text{Volume, cu in}) - 0.151\ (\text{EMC}) + \text{Eq type} \begin{bmatrix} 0 & (\text{Digital}) \\ -2.063 & (\text{Nondig}) \end{bmatrix} \qquad (24)$$

Although coefficient of determination is "fair" in equations (22) and (23), experienced data is within tolerable limits of standard error.

The range of influence on the resultant S-3A test attributes were derived by varying parameters from minimum to maximum to observe the change in MMHI. The results showed that in the case of nondigital electronics, component density and level of fault isolation represented over half of the MMHI:

Component Density, 0.1 to 7.9 comp/cu in	31.1%
Design Ambiguity 62 to 99%	24.3%

No correlation with component density and design ambiguity was noted in the case of digital electronics. This supports the previous observation that the packaging of nondigital electronics tends to be more signal oriented, thus improved functional packaging will tend to reduce the MMHI.

3.2.2 Elapsed Maintenance Time

3.2.2.1 Organizational level. - Low correlation was obtained from multiple regression analysis, therefore the elapsed maintenance time at organizational level (EMTO) is compared in figure 13 and averages 1.4 hours for all equipment. Table 6 shows the individual averages for the 64 S-3A LRUs supported by ATE. Table 10 shows the average for the C-5A LRUs as 1.3 hours for ATE supported units. The P-3C LRUs, tested by ATE at O-Level only, are shown in table 12 and average 2.0 hours. The MK-86 shipboard system, isolated to the SRU level on the weather deck of the ship, averages 4.1 hours. The higher average is accountable for as accessibility to maintenance.

The averages of EMTO for the different systems show that basic maintenance time is the same for different systems, both airborne and ground. This commonality is due to the use of similar types of BIT.

3.2.2.2 Intermediate level. - The elapsed maintenance times at I-Level (EMTI) are also shown in the tables referenced in paragraph 3.2.2.1. The average EMTI for both S-3A and C-5A systems is 3.7 hours. The following relationships were derived from the SPSS analysis:

S-3A Nondigital (R^2 = 0.734, std error = 0.550)

$$\begin{aligned}\text{EMTI} = &- 0.105 + 0.371\ (\text{LNFAIL}) - 0.0005\ (\text{SRUPIN}) \\ &+ 0.0003\ (\text{AEG})\end{aligned} \tag{25}$$

S-3A Digital EMTI had low correlation, Average shown in table 6 is 3.2 hours.

C-5A, ATE and MTE supported, (R^2 = 0.683, std error = 2.415)

$$\begin{aligned}\text{EMTI} = &\ 7.126 + 0.156\ (\text{Weight}) - 0.0026\ (\text{Volume, cu in}) \\ &- 0.150\ (\text{EMC}) + \text{Equip. Type} \begin{bmatrix} 0\ (\text{Digital}) \\ -2.291\ (\text{Nondig}) \end{bmatrix}\end{aligned} \tag{26}$$

Comparison of the EMTI for S-3A of 3.2 hours to the average computed run time (RUNPRED) in table 5 of 1.3 hours reveals that more reduction can be expected in the 1977 averages as the optimized software test programs developed in 1978 and 1979 are deployed. Recent comparison shows a reduction of 50 percent in the first units, thus the RUNPRED is a realistic goal for future predictions.

3.2.3 ATE versus MTE

The data presented in table 6 (S-3A, ATE), table 8 (S-3A, MTE), and table 10 (C-5A) are shown in figures 14 and 15. Figures 14 and 15 show that O-Level averages for all systems are essentially the same, since the same method of BIT support is used. Figure 14 shows the I-Level average MTE maintenance manhours is 15.1 percent over ATE (MMHI). Therefore, the data base shows an improvement using ATE as:

$$\Delta MMHI_{ATE} = \frac{9.3 \text{ hrs ATE}}{10.7 \text{ hrs MTE}} = 0.869 \text{ of MTE}$$

Figure 15 shows the I-Level average MTE elapsed maintenance time is 141 percent over ATE (EMTI). Therefore, the data base shows an improvement using ATE as:

$$\Delta EMTI_{ATE} = \frac{3.7 \text{ hrs ATE}}{8.9 \text{ hrs MTE}} = 0.416 \text{ of MTE}$$

The conclusion drawn is that EMT can be expected to be less than one half the average elapsed time using ATE in lieu of MTE.

3.2.4 Airborne versus Ground

The comparison of the MK-86 shipboard equipment, shown in figure 14 resulted in a 4.1 hour average, which compares to the total average for both S-3A and C-5A systems of 4.9 hours. The MK-86 O-Level support uses a combination of BIT and operator actions to isolate to the SRU level of repair. This represents the same level of activity required at the two levels of airborne equipment to accomplish the SRU level isolation. With the limited data available, it is assumed that airborne and ground equipment require the same level of maintenance to effect isolation to the SRU level of repair.

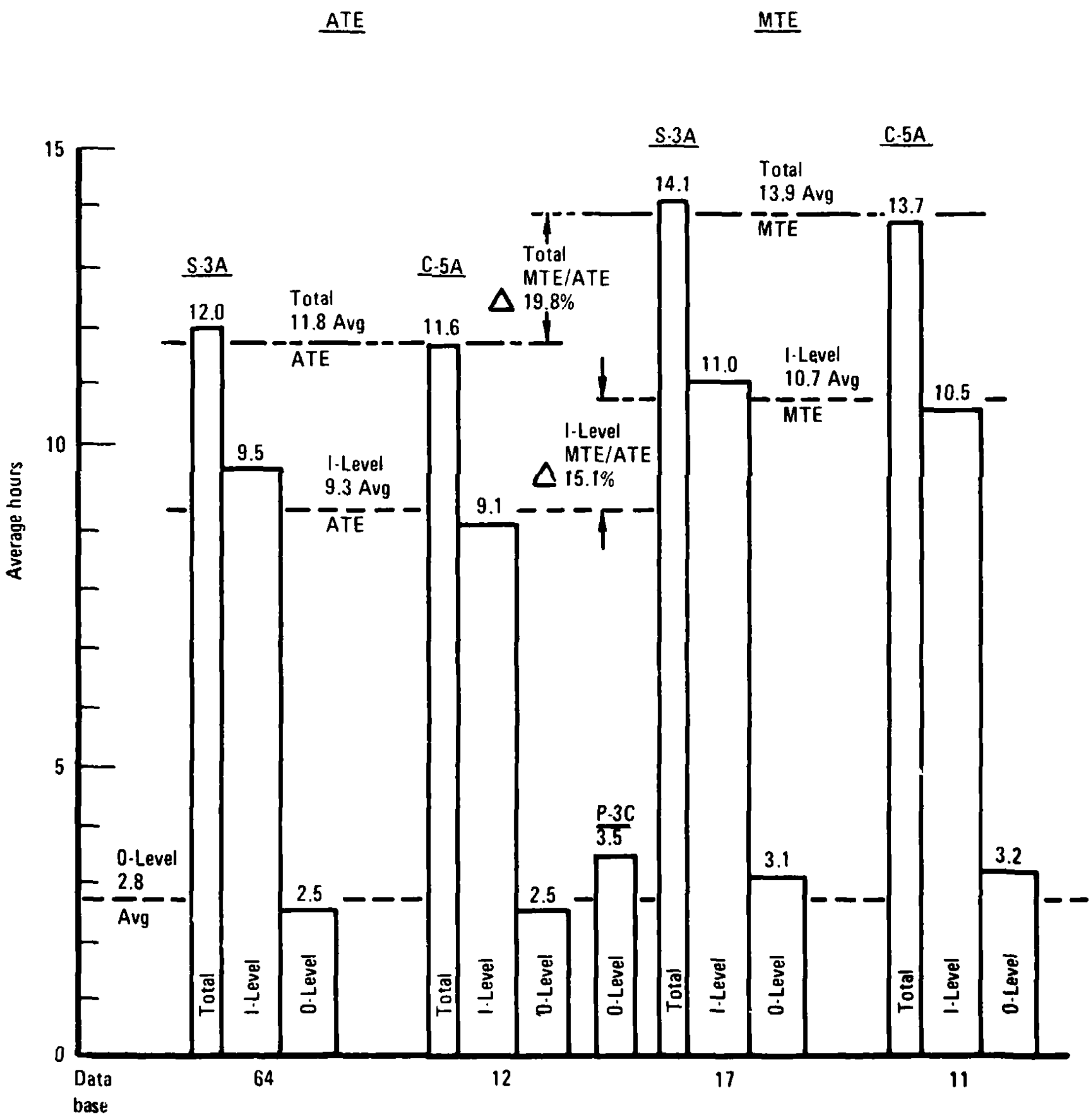


Figure 14. - Comparison of ATE and MTE S-3A and C-5A airborne equipment maintenance manhours.

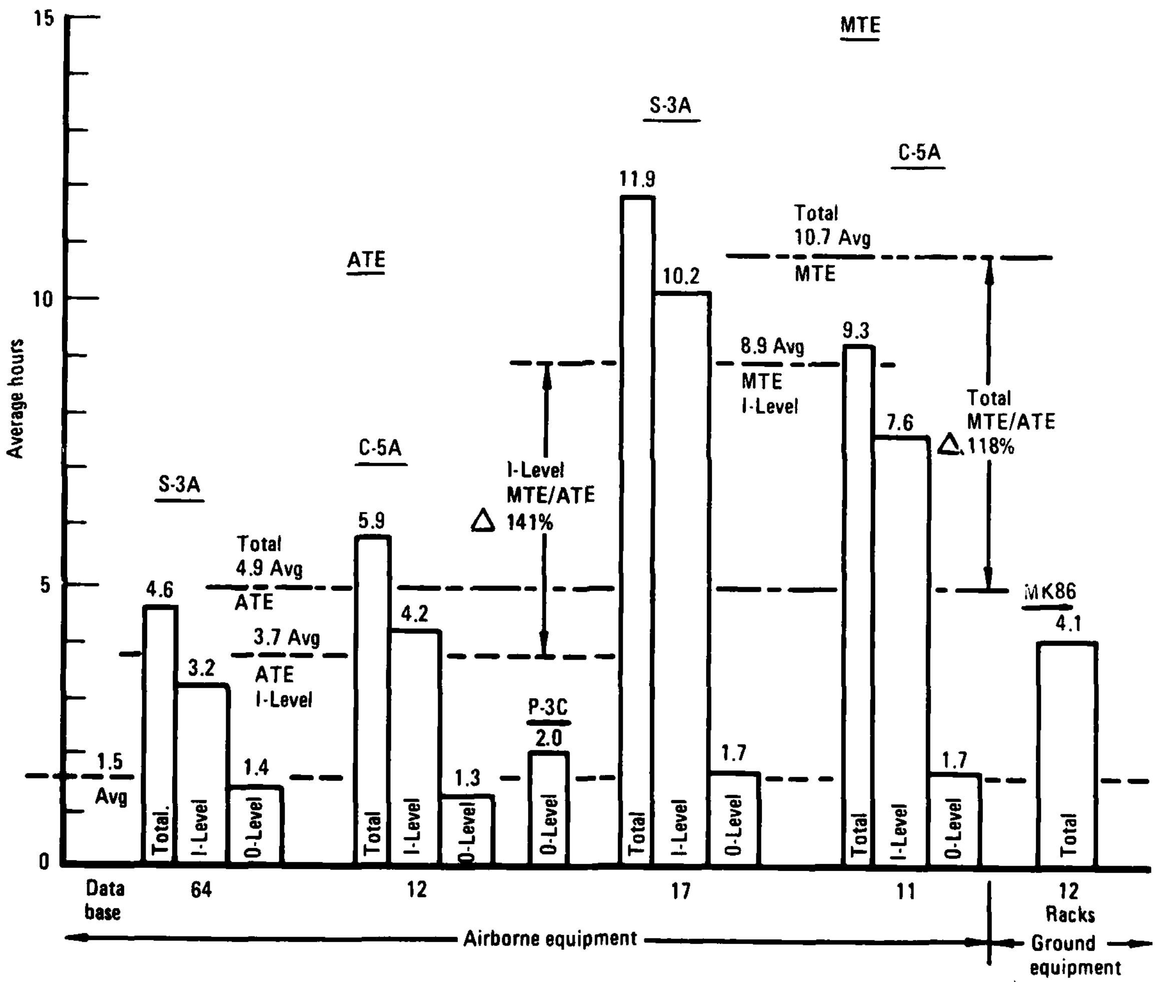


Figure 15. - Comparison of ATE and MTE, S-3A, C-5A and MK-86 equipment-elapsed maintenance time.

4. TRADEOFF CRITERIA

The analysis shown in section 3 can be used to predict the life cycle cost elements of the test subsystem from the Unit-Under-Test (UUT) design characteristics.

The equipment design characteristics can be used to predict the least support costs which will meet the specified system availability. As an example, assume that a decision must be made between manual test equipment (MTE) or Automatic Test Equipment (ATE) support. Assume that the following UUT characteristics are known:

During preliminary development phase:

Non-digital LRU
Number of SRUs = 19
Number of I/O pins = 300
Weight = 27lbs
Volume = 1330 cu in
Estimated input power = 600 watts
Predicted MTBF = 450 hours

After CDR (Critical Design Review), the LRU is more definitive and has the following additional characteristics:

1. The number of unique functional submodules is 19, and there is an additional penalty count of one for a data multiplexer (see para. 2.2.1), or an equivalent module count (EMC) of 20.

2. Examination of the test requirement documentation (TRD) shows, that from the UUT schematic and parts list, the component elements are as follows:

    total SRU pins = 921 (SRUPIN)
    total I/O pins = 316 (LRUPIN)
    active circuit count = 1009 (AEG)
    (see fig. 11)

Number of components = 260 (COMP)

Computed failure modes = 950 (FAILMODE)
(see para. 2.2.1)

Natural Log of failure modes = 6.9 (LNFAIL)

3. Evaluation of the UUT has resulted in the following additional requirements:

UUT/ATE interface components = 20

UUT/ATE interface active circuits = 2 AF^

Functional modularity = nominal

Circuit type = discrete

4. Mission Requirements

Operating hours per quarter = 450 hrs

Fault isolation to one SRU = 90%

Preliminary estimates of maintenance time must be based on averages per table 6:

MMHI = 8.0 hours

EMTI = 3.2 hours

$$\text{Crew size} = \frac{\text{MMHI}}{\text{EMTI}} = \frac{8.0}{3.2} = 2.5$$

From the data base, the savings in I-Level maintenance time is predicted (paragraph 3.2.3) as:

$$\Delta\,\text{EMTI}_{\text{ATE}} = 0.416 \text{ of MTE time}$$

$$\text{EMTI}_{\text{ATE}} = 3.2 \text{ hours (est)}$$

$$\text{EMTI}_{\text{MTE}} = \frac{3.2}{.416} = 7.7 \text{ hrs (est)}$$

As a check on preliminary information, equation (26) can be used to compare expected EMTI from UUT characteristics:

$$EMTI = 7.126 + 0.156\ (WEIGHT) - 0.0026\ (VOL) - 0.15\ (EMC) - 2.291\ (NON\text{-}DIG.\ type)$$

$$= 7.126 + 0.156\ (27) - 0.0026\ (1330) - 0.15\ (19) - 2.291$$

$$= 2.739 \text{ hours}$$

Since equation (26) represents a combination of ATE and MTE, the forecasted average of 3.2 hours for ATE and 7.7 hours for MTE are reasonable for early predictions.

The predicted number of maintenance actions is computed. The MTBMA equals MTBF for the case of no scheduled maintenance. The number of intermediate level maintenance actions per quarter is:

$$\text{No. of actions} = \frac{500 \text{ operating hours}}{450 \text{ MTBMA}}$$

$$= 1.1 \text{ actions per system}$$

In 10 years the number of hours saved using ATE in lieu of MTE would be 40 quarters times 1.1 actions times 4.5 hours per action (7.7 minus 3.2), or 198 hours per system. The cost of developing an ATE program to realize this savings is computed from the preliminary UUT characteristics from equation (18) as:

$$TPSHRS = 609 + 150\ (EMC) + 3.69\ (LRUPIN)$$

$$= 609 + 150\ (19) + 3.69\ (300)$$

$$= 4566 \text{ hours}$$

In this calculation, EMC is equated to the 19 SRUs and LRUPINS to the estimate I/O pin count. To evaluate the return on investment of 198 test hours saved per system and the crew size of 2.3 are used. Savings is the TPSHRS divided by the savings per system and crew size:

$$\frac{4566}{198X2.3} = 10.0 \text{ systems to break even}$$

After CDR, a more accurate prediction of cost savings can be made. The design coefficients are determined from paragraph 3.1.1.1:

- Interface compatibility (IDVAL)

$$IDVAL = IDAEG + IDCOMP/50 + LRUPIN/100$$
$$= 2 + 20/50 + 316/100 = 5.6 \text{ (simple)}$$

$$K_{TC} = 0.000$$

- Functional Modularity, degree of packaging, nominal

$$K_{MOD} = 0.005$$

- Circuit type, at least 75% discrete components

$$K_{CKT} = 0.156$$

- Components per cu. in. ≐ COMP/VOL

$$= 260/1330 = 0.19$$

$$K_{DENS} = 0.000$$

- Fault Isolation 90% to one SRU

$$K_{ISOL} = 0.078$$

From equation (14):

$$K_D = \frac{1}{1-(K_{TC} + K_{MOD} + K_{CKT} + K_{DENS} + K_{ISOL})}$$

$$= \frac{1}{1-(0 + 0.005+0.156+0+0.078)} = 1.31$$

TPS Development Costs, equation (16):

$$TPSHRS = K_D \left[-2143+0.315(COMP)+55.2(EMC)+519 \ (LNFAIL)+2.018(LRUPIN) \right]$$

$$= 1.3.1 \left[-2143+0.315 \ (260) + 55.2 \ (20)+519 \ (6.9) + 2.018 \ (316) \right]$$

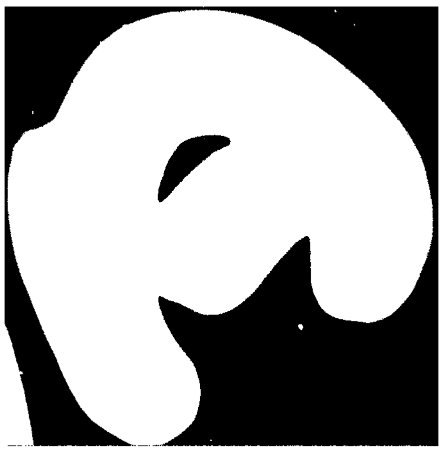
$$= 4273 \text{ hours}$$

The maintenance manhours (MMHI) are computed from equation (23):

$$MMHI = -5.421 + 1.888 \ (LNFAIL)$$
$$= -5.421 + 1.888 \ (6.9) = 7.6 \text{ hrs.}$$

From equation (25), EMTI is computed:

$$EMTI = -0.105+0.371(LNFAIL)-0.0005(SRUPIN)+0.0003(AEG)$$
$$= -0.105+0.371(6.9)-0.0005(921)+0.0003(1009)$$
$$= 2.3 \text{ hrs.}$$



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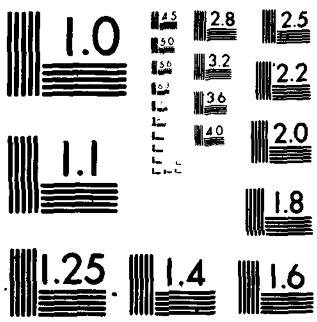

MICROCOPY RESOLUTION TEST CHART

To evaluate the return on investment of TPSHRS for ATE savings, the savings using final UUT characteristics is computed:

$$MMHI = 7.6 \text{ hrs}$$
$$EMTI = 2.3 \text{ hrs}$$
$$\text{crew size} = 7.6/2.3 = 3.3$$
$$TPSHRS = 4273 \text{ hrs}$$

If MTE were used, the average elapsed maintenance time would be

$$EMTI_{MTE} = \frac{EMTI_{ATE}}{.416} = \frac{2.3}{.416}$$
$$= 5.5 \text{ hrs}$$

The 0.416 rate is derived from the data base. The savings in time is 5.5 - 2.3 = 3.2 hours. Using the same number of maintenance actions as derived earlier for MTBMA, the 10 year savings would be 1.1 actions per system times 40 quarters (10 years) times 3.2 hours saved per action, or 140.8 hours per system.

The return on investment of 140.8 hours saved per system is:

$$\frac{4273}{140.8 \times 3.3} = 9.2 \text{ systems to break even}$$

This result compares to the value of 10.0 computed from preliminary data. In this example the cost of TPS development would pay off in maintenance cost savings for a prime system which supports more than 10 LRUs. If for example 100 LRUs are to be supported for ten years, the savings would be (100-10) X 140.8 hrs per LRU which is a savings of 12,672 hours per TPS design.

Similar calculations for other situations can be made from the algorithms developed in this study.

5. CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

The following generalizations can be made from the results of the study:

- The cost of maintenance of electronic equipment can be predicted from the Unit-Under-Test (UUT) design characteristics.

- The use of Built-In-Test (BIT) is mandatory to maintain the low cost of organizational level support as the electronics becomes more compact.

- The development of ATE test programs will equal the savings in maintenance manhours over a ten year life cycle cost. The cost of maintenance saved can be computed from the algorithms developed in this study.

5.2 Recommendations

The findings of this study were limited in scope to obtain the maximum practical data from the contracted expenditures. The data base as a result was only partially explored. One extension to the study would be to explore more data points on the four systems in the study, particularly in the area of component and failure mode count so that more organizational level predictions can be derived. A second extension would be the study of the submodule cost trade-offs. A third would be to derive the weighting factors to more accurately predict actual non-ambiguity ratios experienced in the actual rates.

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ABBREVIATIONS AND DEFINITIONS

Abbreviations

A	-	*Availability
AEG	-	*Active Element Group (component of a SRU)
AMBDES	-	Variable, percent of fault isolation to a single SRU - design demonstration
AMBACT	-	Variable, actual fault isolation ambiguity to one SRU - field experience
ATE	-	Automatic Test Equipment
ATLAS	-	Abbreviated Test Language for Avionics Systems
BIT	-	*Built in test
BITE	-	*Built in test Equipment
CND	-	Cannot Duplicate
COMP	-	Components, the number in a unit
DFC	-	Diagnostic Flow Chart
EMC	-	*Equivalent Module Count
EMT	-	Elapsed Maintenance Time
EMTI	-	EMT at Intermediate Level
EMTO	-	EMT at Organizational Level
FUNCMOD	-	*Functional modularity
ID	-	Interconnection Device (between test equipment and UUT)
I/O	-	Input and/or Output Interface
I-Level	-	*Intermediate Level Maintenance
K_D	-	Design coefficient of testability
LCC	-	Life Cycle Cost
LNFAIL	-	The natural logarithm of the number of failure modes in a unit
LOR	-	Level of Repair
LRU	-	*Line Replaceable Unit
LRUPIN	-	The number of active I/O pins at the LRU interface
MMH	-	Maintenance Manhours

*Definitions are listed below

MMHI	-	MMH at Intermediate Level
MMHO	-	MMH at Operational Level
MTE	-	Manual Test Equipment
MTBF	-	Mean Time Between Failures - generic failure rate
MTBMA	-	Mean Time Between Maintenance Actions - experienced failure rate
MTBUR	-	Mean Time Between Unscheduled Removals
MTTR	-	Mean Time to Repair
NRTS	-	Non-Repairable Test Subsystem
O-Level	-	*Organizational Level Maintenance
OR	-	Operational Readiness
RFI	-	Ready for Issue
R&R	-	Remove and Replace
R^2	-	Coefficient of Determination
SN-AR	-	Shop Non-Ambiguity Ratio
SRU	-	*Shop Replaceable Unit
SRUPIN	-	The total number of active SRU pins in a LRU
SSRU	-	*A submodule of SRU
STAHRS	-	Number of stations hours required in TPS development
TE	-	Test Equipment
TPI	-	Test Program Instructions
TPS	-	*Test Program Set
TPSHRS	-	Test Program Set Development manhours
TRA	-	Test Requirement Analysis
TRD	-	*Test Requirement Document
UUT	-	Unit-Under-Test

*Definitions are listed below

Definitions

Availability - The attribute of the equipment to perform its intended mission, express in percent of time it is able to perform.

Active Element Group - The number of active stages in an electronic unit. An active stage is defined as a transistor, diode bridge, or equivalent stages of circuitry in an integrated circuit.

Built-In Test (BIT) - Electronics system Self test used in organizational and in-flight testing, utilizing BITE.

Built-In Test Equipment (BITE) - Any device or circuit permanently mounted in the equipment and used for the express purpose of testing, either independently or in association with external sources.

Depot Level Maintenance - Maintenance which requires the return of certain segments of a system or equipment to a depot (Rework Facility) or contractor facility for repair, rework, alterations, or overhaul.

Equivalent Module Count - The number of replaceable modules or submodules in a unit with allowance for test complexity and commonality.

Functional Modularity - The degree of modularity both physical and electrical of a given unit.

Intermediate Maintenance (Shop) - All maintenance, other than organizational maintenance, performed for direct support of the using activity, employing only skills, tools, support equipments, publications, procedures, techniques, and shop facilities planned for normal service use at a designated intermediate maintenance facility.

Line Replaceable Unit (LRU) - A generic term which includes all the replaceable packages of an avionic equipment or system as installed in an aircraft system, with the exception of cables, mounting provisions, and fuse boxes or circuit breakers. Conversely, a system or set is composed entirely of LRU's, plus cabling, mounting provisions, fuse boxes or circuit breakers.

Orginizational Maintenance (Flight Line) - All maintenance performed by the using organization employing all those skills, tools, support equipments, publications, procedures, and techniques planned for service use when deployed.

Test Program Set - Complete software package including test tape or disc, supporting documentation, and associated interconnection cabling and devices. See MIL-STD-2077 (AS).

Test Requirements Document - All documentation required to define test procedures for the UUT, which includes ATE compatibility reports, diagnostic flow charts, test diagrams, interface requirements, etc. See MIL-STD-2076 (AS).

Definitions (Continued)

Shop Replaceable Unit (SRU) - A generic term which includes all the packages within a LRU, including chassis and wiring as a unit. Conversely, a LRU is composed entirely of SRU's.

Shop Replaceable Unit (SSRU) - A modular unit which is packaged inside an SRU. All indices and test point requirements applicable to SRU's are also applicable to SSRU's. All calculations should be made the same as if the SSRU were and SRU and the SRU were a LRU.

TERMINOLOGY

Systems/Components	US Army and US Air Force	US Navy
Replaceable Unit	Line Replaceable Unit (LRU)	Weapons Replaceable Unit (WRA)
Submodule	Sub Replaceable Unit (SRU)	Shop Replaceable Assembly (SRA)
Subassembly	SSRU	SSRA

TABLE OF NATURAL LOG FUNCTIONS

N	LN (N)	N	LN (N)
100	4.6	8000	9.0
200	5.3	10K	9.2
400	6.0	12K	9.4
500	6.2	15K	9.6
600	6.4	20K	9.9
800	6.7	22K	10.0
1000	6.9	25K	10.1
1100	7.0	27K	10.2
1500	7.3	30K	10.3
2000	7.6	40K	10.6
2500	7.8	50K	10.8
3000	8.0	60K	11.0
4000	8.3	80K	11.3
5000	8.5	100K	11.5
6000	8.7		

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